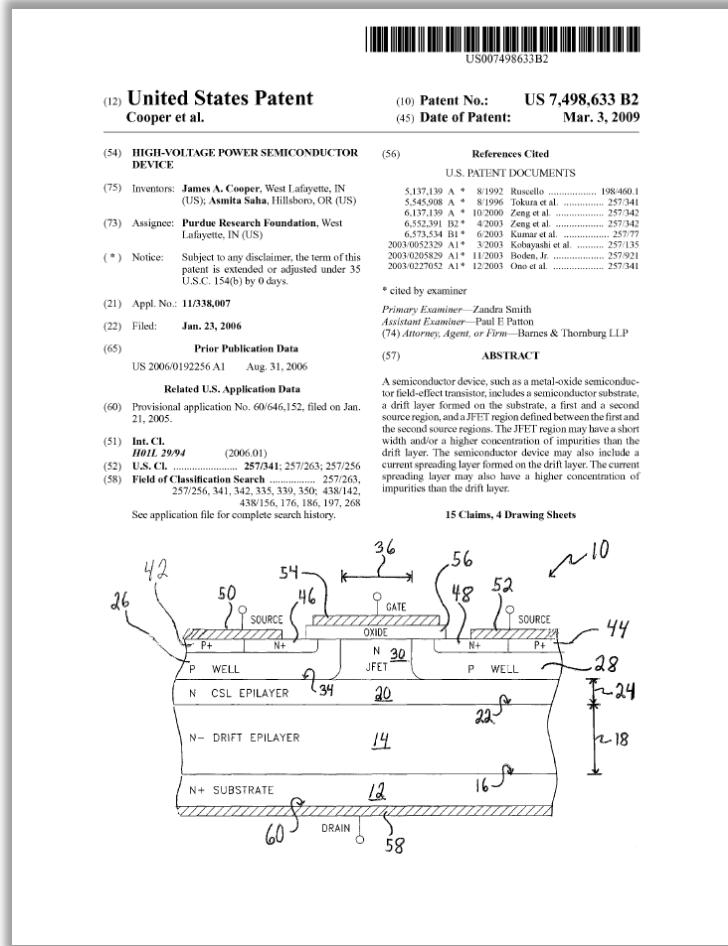


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# EXHIBIT C

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**Title: HIGH-VOLTAGE POWER SEMICONDUCTOR DEVICE**

**Priority Date:** Jan. 21, 2005

**Filed Date:** Jan. 23, 2006

**Issued Date:** Mar. 03, 2009

**Expiration Date:** Jan. 23, 2026

**Inventors:** James A. Cooper; Asmita Saha

**Exemplary Claim:** 9

### Claim 9

A **double-implanted metal-oxide semiconductor field-effect transistor** comprising:

- a **(SUB) silicon-carbide substrate**;
- a **(DL) drift semiconductor layer** formed on a **(FS) front side** of the **(SUB) semiconductor substrate**;
- a **(FS) first source region**;
- a **(FSE) first source electrode** formed over the **(FS) first source region**, the **(FSE) first source electrode defining a longitudinal axis**;
- a **(FBC) plurality of first base contact regions** defined in the **(d) first source region**,  
**(FBC) each of the plurality of first base contact regions being spaced apart from each other** in a **(FSE) direction parallel to the longitudinal axis defined by the first source electrode**;
- a **(SS) second source region**;
- a **(SSE) second source electrode** formed over the **(SS) second source region**, the **(SSE) second source electrode defining a longitudinal axis**;
- a **(SBC) plurality of second base contact regions** defined in the **(SS) second source region**,  
**(SBC) each of the plurality of second base contact regions being spaced apart from each other** in a **(SSE) direction parallel to the longitudinal axis defined by the second source electrode**; and
- a **(JF) JFET region** defined between the **(FS) first source region** and the **(SS) second source region**,  
**the (JF) JFET region having a width less than about three micrometers**.

Claim 9

A double-implanted metal-oxide semiconductor field-effect transistor comprising:

**SCTW90N65G2V**  
Datasheet

Silicon carbide Power MOSFET 650 V, 119 A, 18 mΩ (typ.,  $T_J = 25^\circ\text{C}$ )  
in an HiP247 package

**Features**

Order code	$V_{DS}$	$R_{DS(on)} \text{ max.}$	$I_D$
SCTW90N65G2V	650 V	24 mΩ	119 A

- Very high operating junction temperature capability ( $T_J = 200^\circ\text{C}$ )
- Very fast and robust intrinsic body diode
- Extremely low gate charge and input capacitances

**Applications**

- Switching applications
- Power supply for renewable energy systems
- High frequency DC-DC converters

**Description**

This silicon carbide Power MOSFET device has been developed using ST's advanced and innovative 2<sup>nd</sup> generation SiC MOSFET technology. The device features remarkably low on-resistance per unit area and very good switching performance. The variation of switching loss is almost independent of junction temperature.

HiP247

G(1)

D(2, TAB)

S(3)

AMD1475v1\_noZen

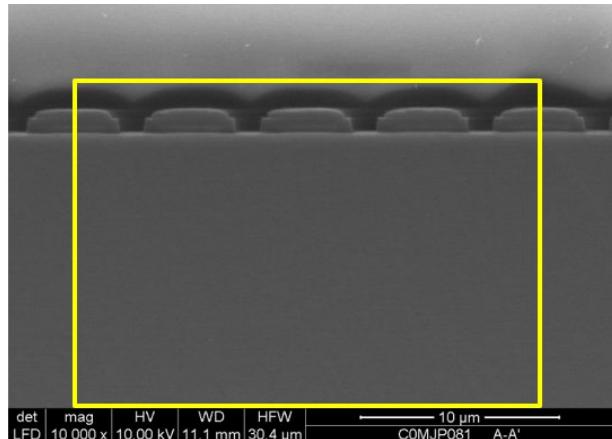
Claim 9

A double-implanted metal-oxide semiconductor field-effect transistor comprising:

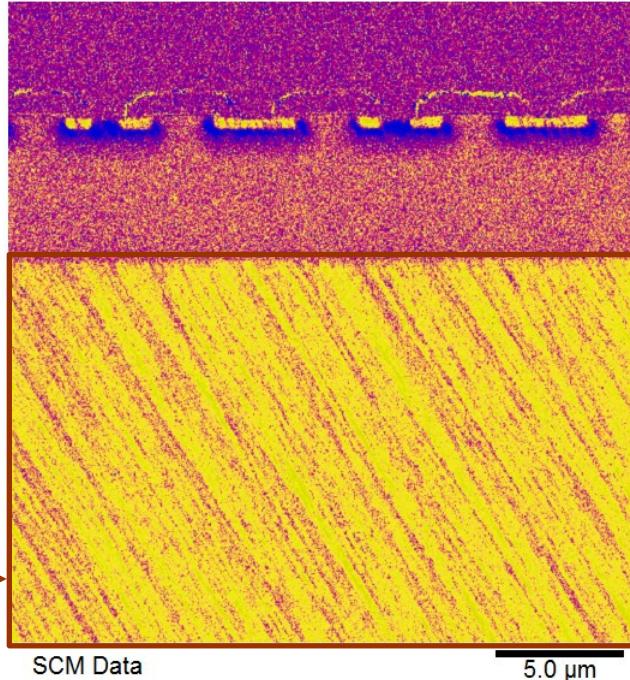


Claim 9

a (SUB) silicon-carbide substrate;



SEM



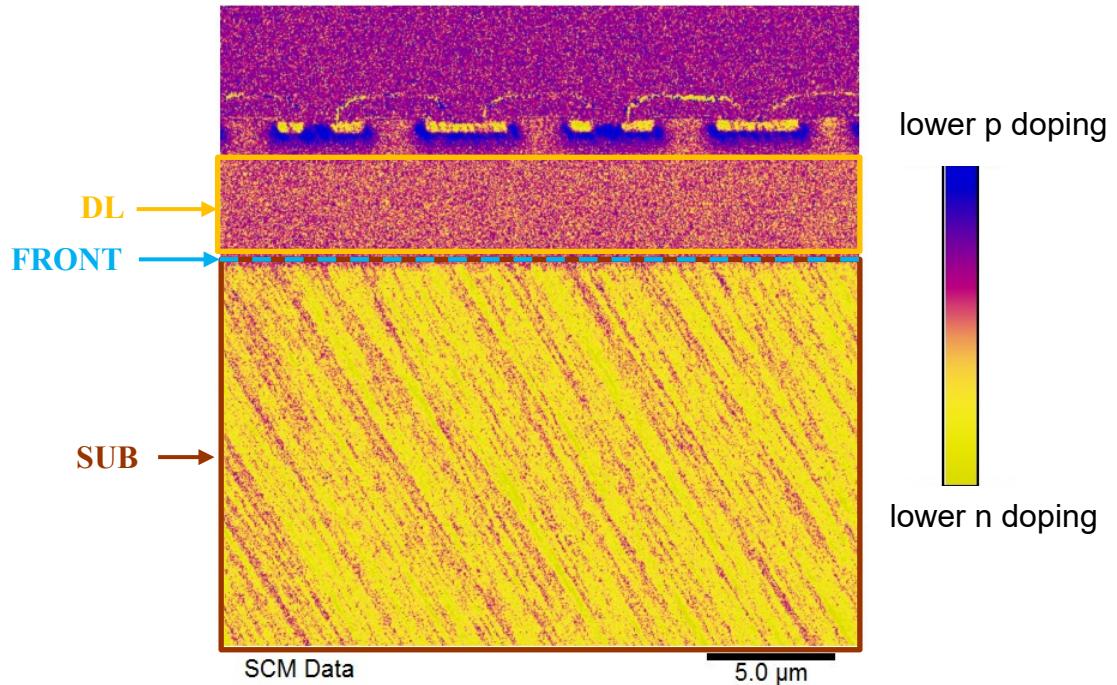
lower p doping

lower n doping

**Note:** Scanning Capacitance Microscopy (SCM) taken of the framed area in the Scanning Electron Microscopy (SEM) image

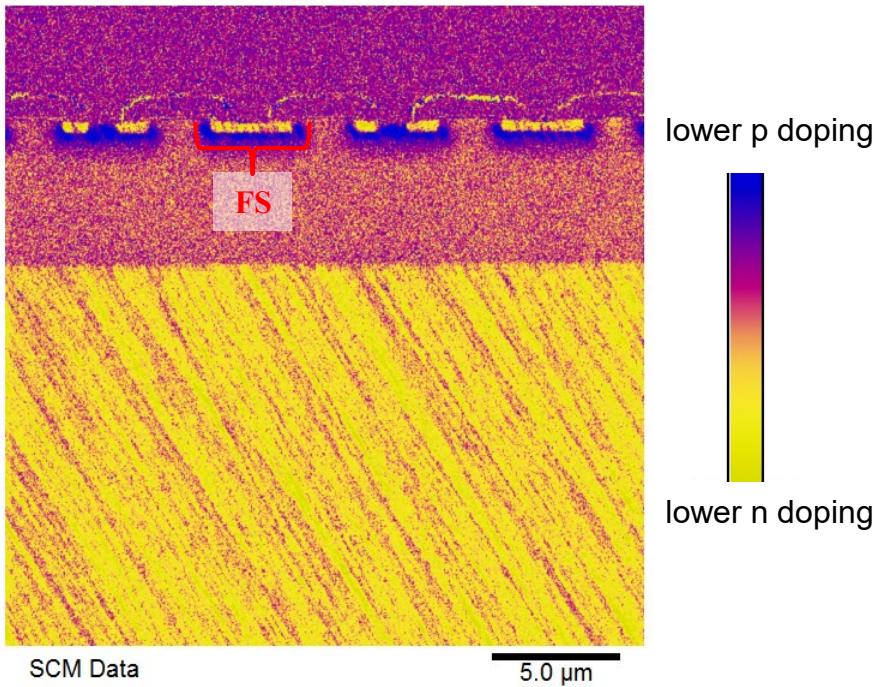
Claim 9

a (DL) drift semiconductor layer formed on a (FRONT) front side of the (SUB) semiconductor substrate;



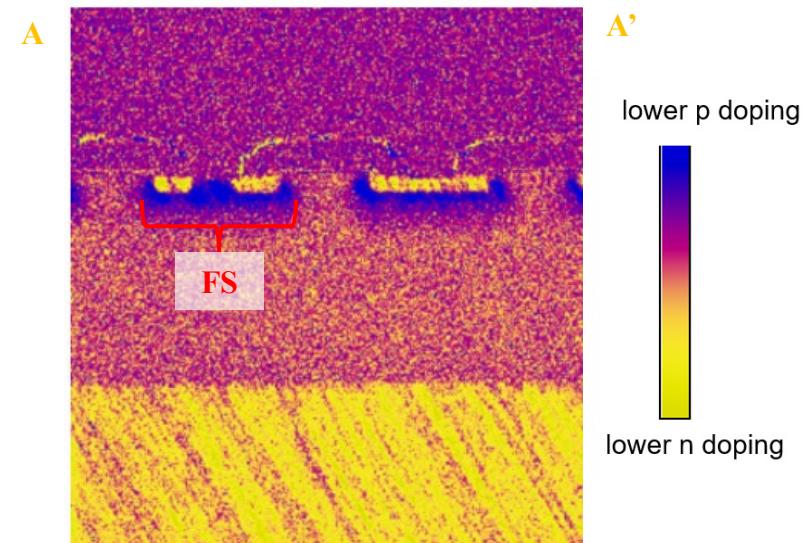
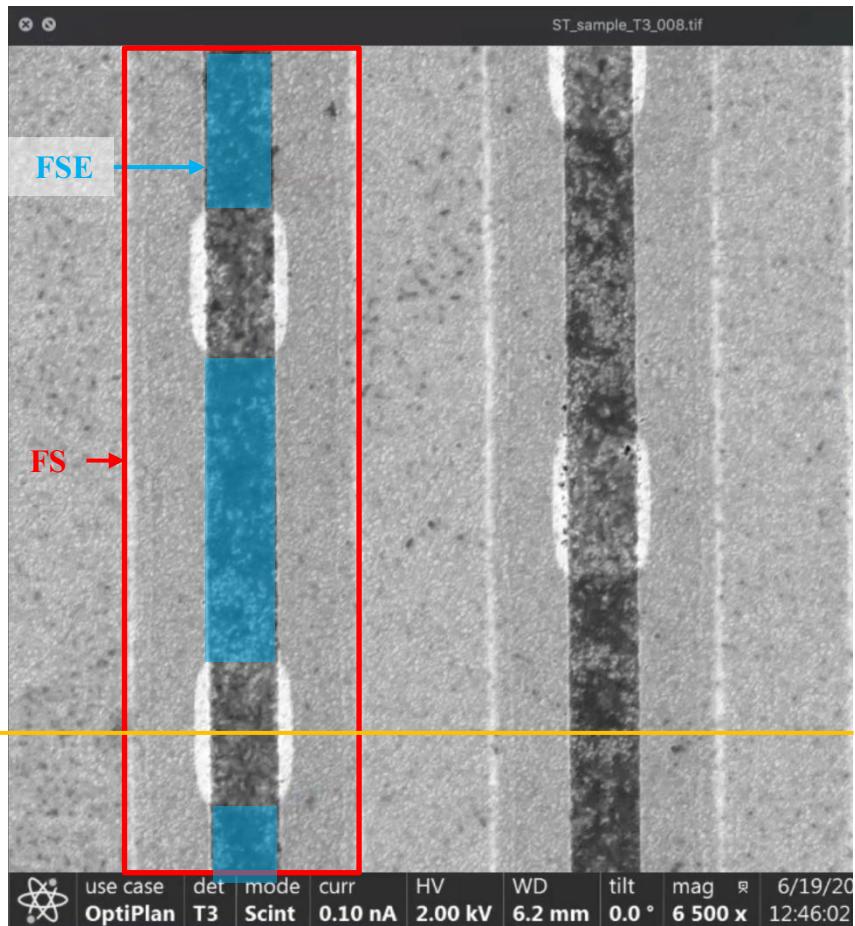
Claim 9

a (FS) first source region;



## Claim 9

a (FSE) first source electrode formed over the (FS) first source region, the (FSE) first source electrode defining a longitudinal axis;

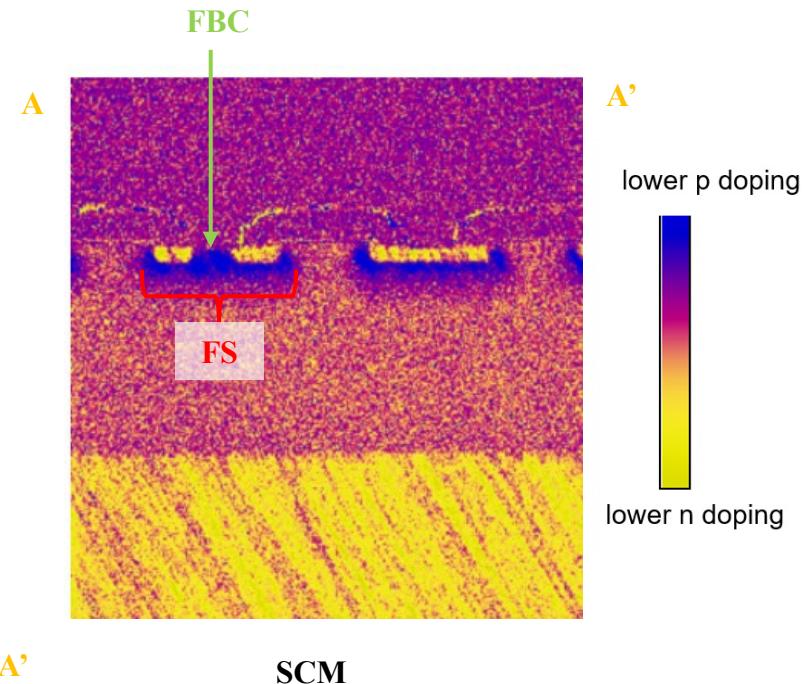
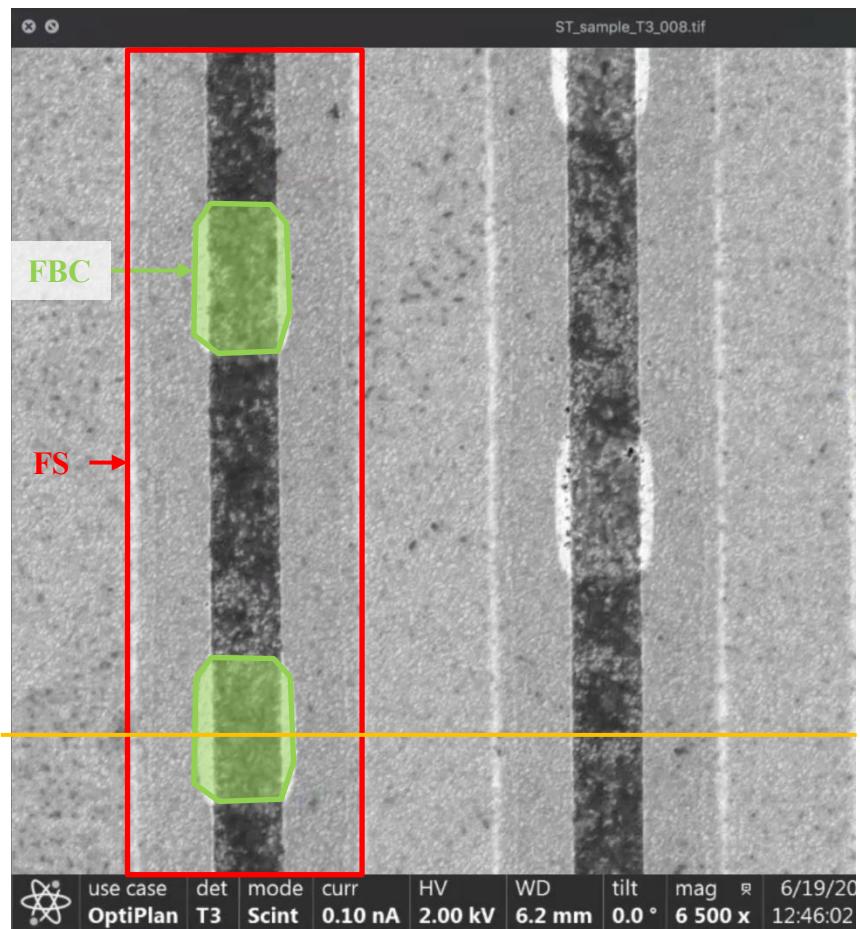


**Note:** SCM view taken at the A-A' cross section

**Note:** Top-down view using Scanning Electron Microscopy Secondary Electron Potential Contrast (SEM SEPC), after polishing down to the silicon carbide.

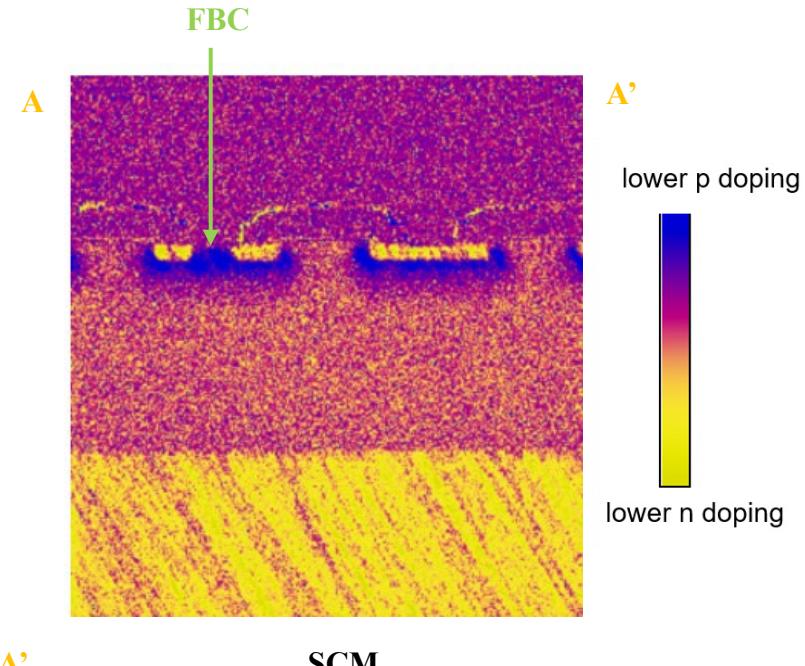
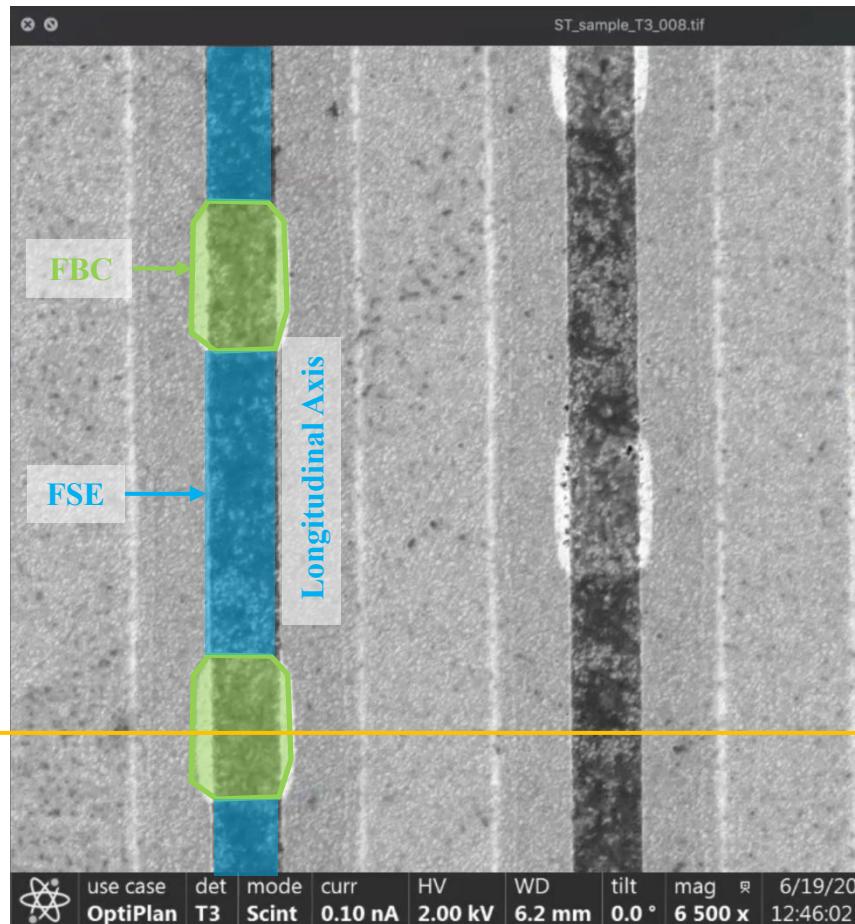
Claim 9

a (FBC) plurality of first base contact regions defined in the (FS) first source region,



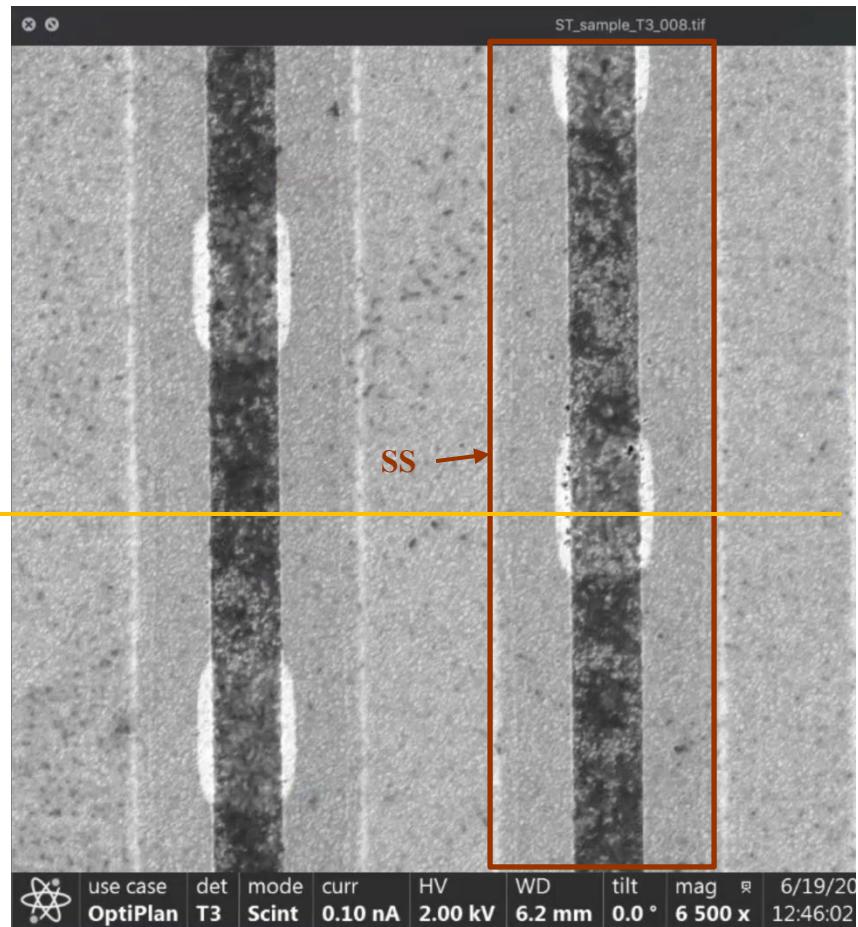
Claim 9

(FBC) each of the plurality of first base contact regions being spaced apart from each other in a (FSE) direction parallel to the longitudinal axis defined by the first source electrode;

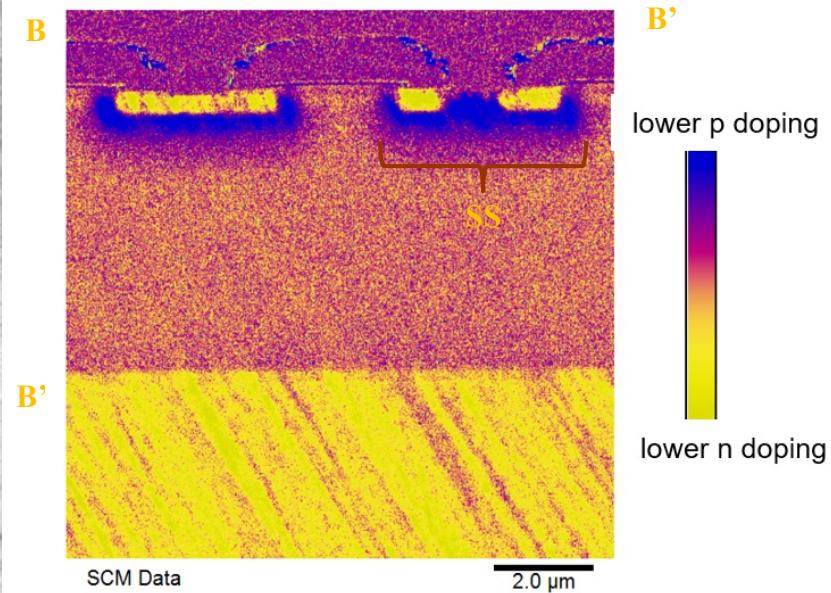


Claim 9

a (SS) second source region;



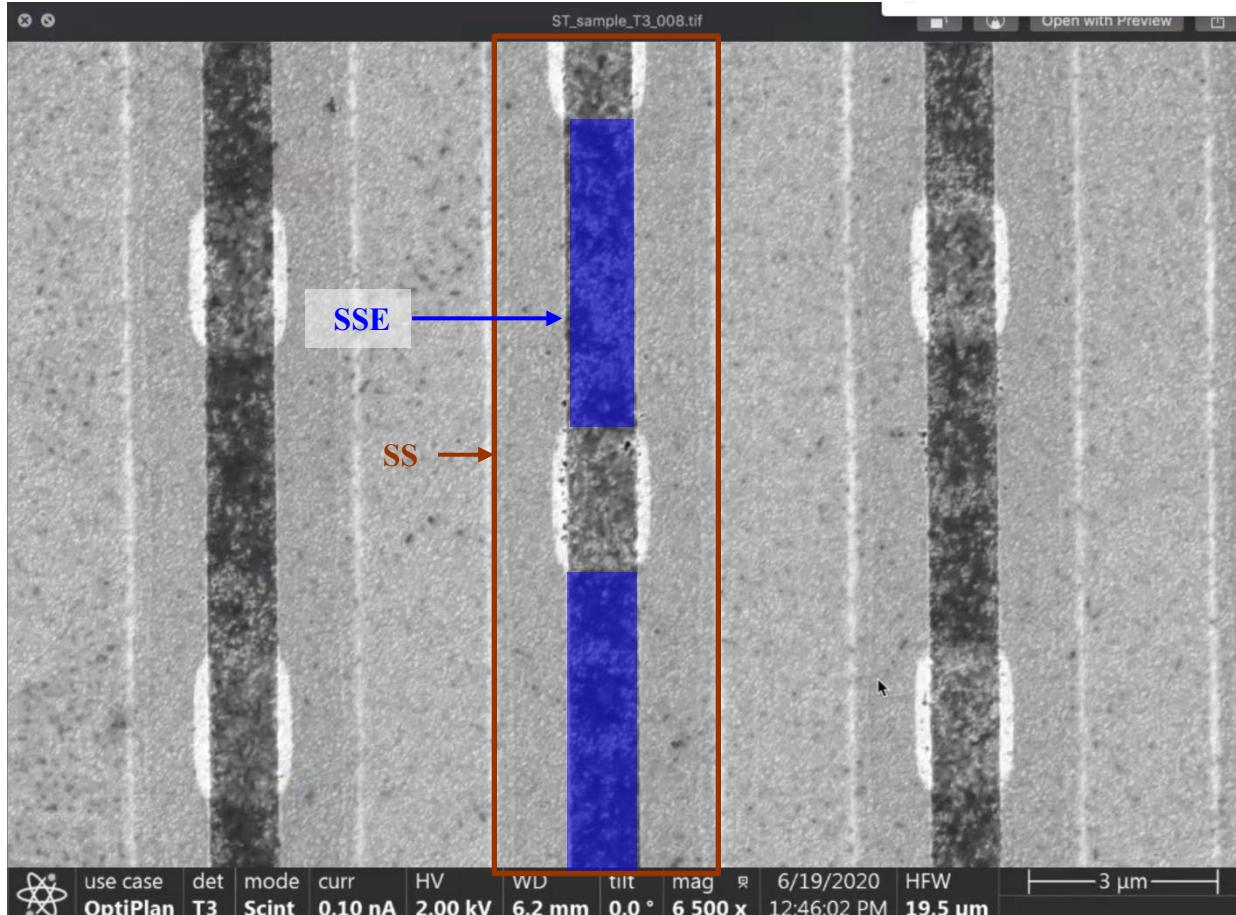
SEM SEPC



Note: SCM view taken at the B-B' cross section

Claim 9

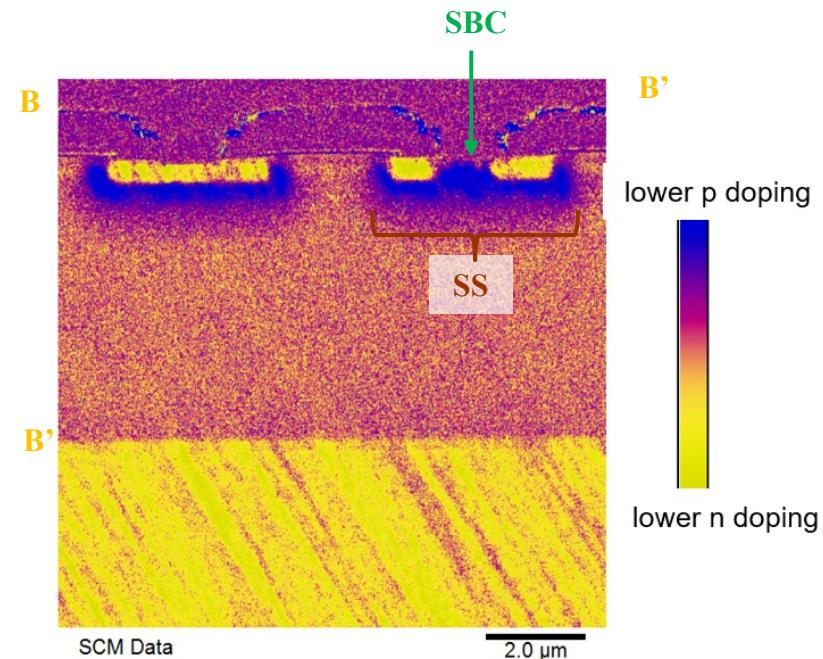
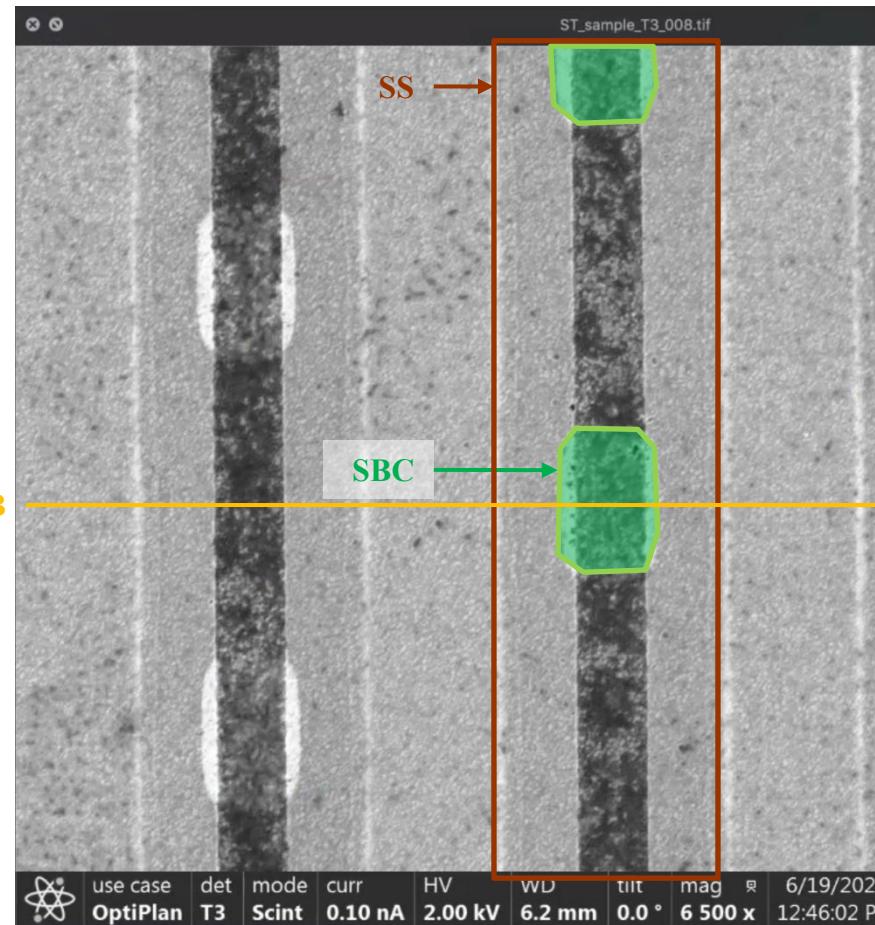
a (SSE) second source electrode formed over the (SS) second source region, the (SSE) second source electrode defining a longitudinal axis;



SEM SEPC

Claim 9

a (SBC) plurality of second base contact regions defined in the (SS) second source region,

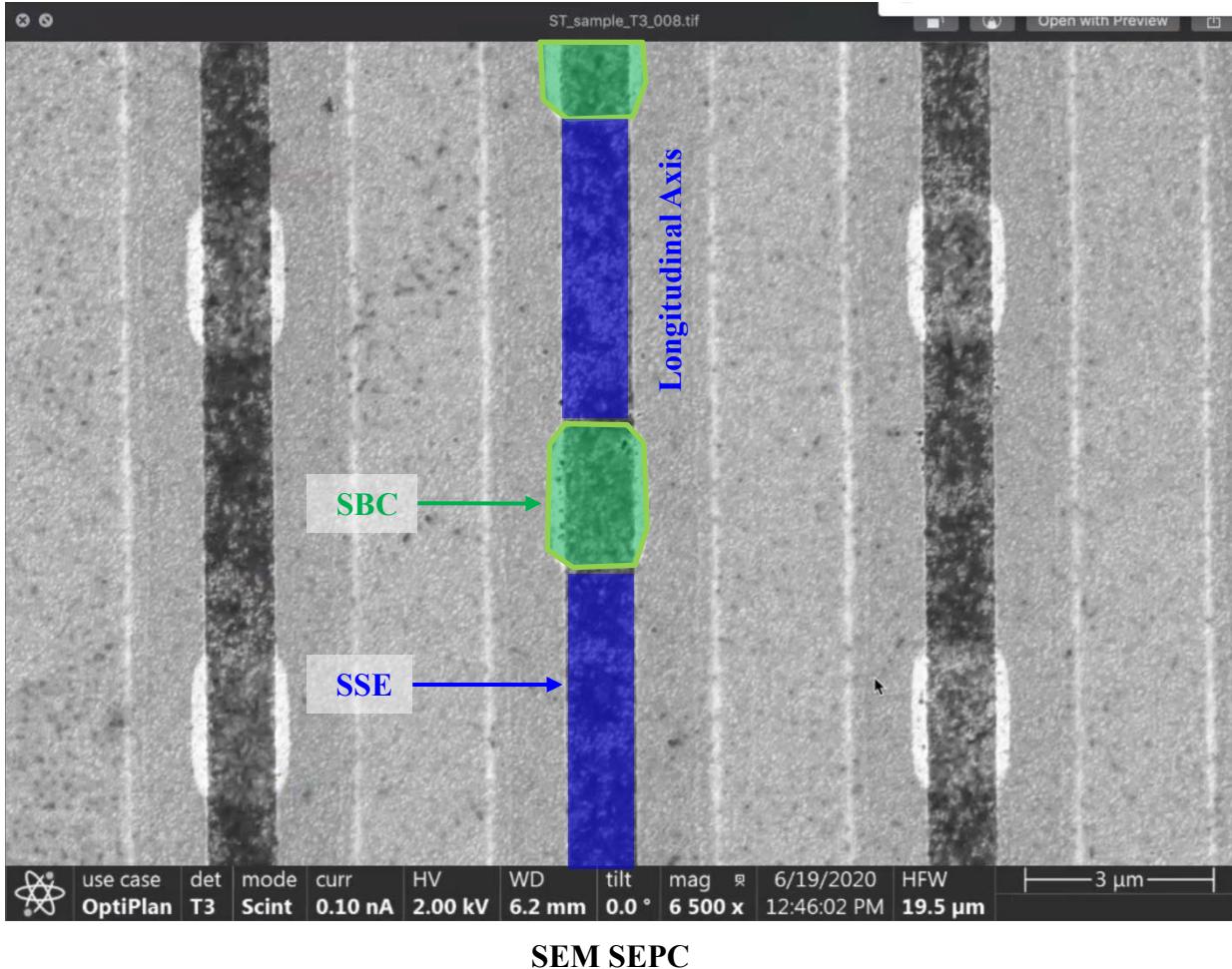


Note: SCM view taken at B-B' cross section

SEM SEPC

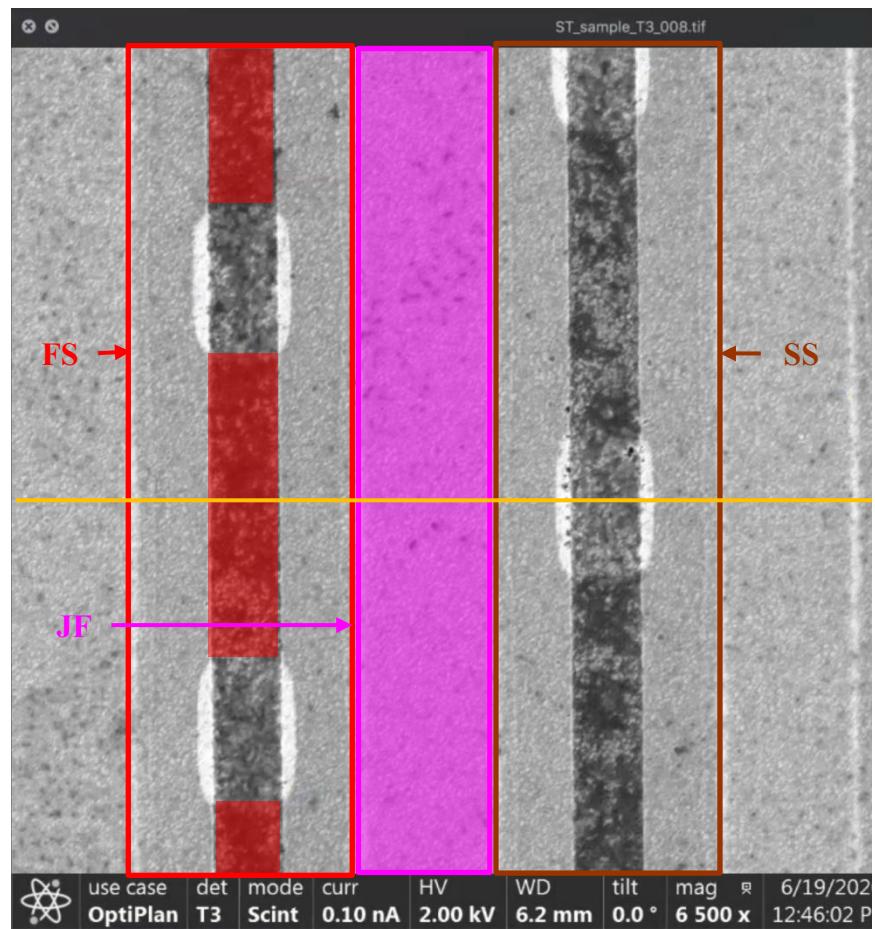
Claim 9

(SBC) each of the plurality of second base contact regions being spaced apart from each other in a (SSE) direction parallel to the longitudinal axis defined by the second source electrode; and

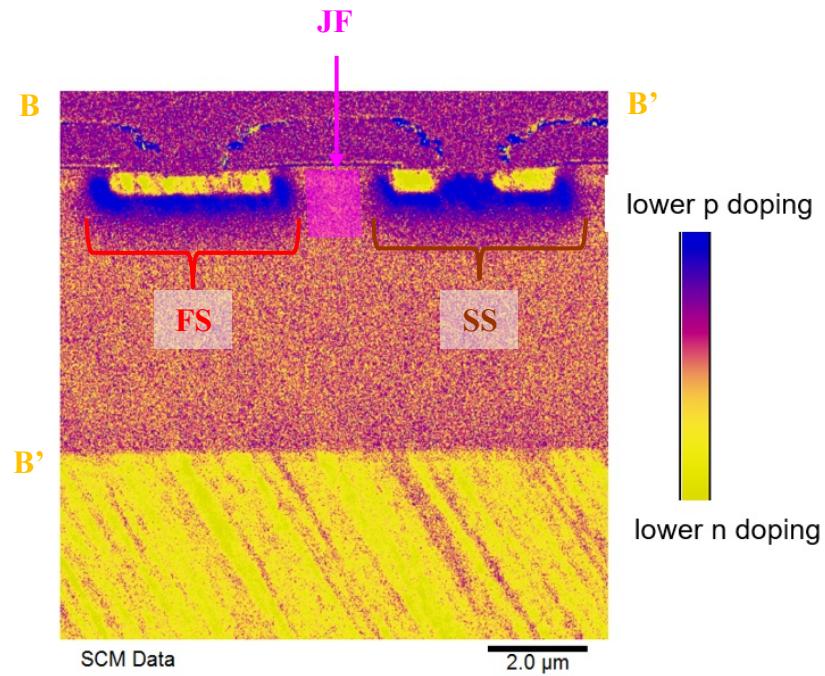


Claim 9

a (JF) JFET region defined between the (FS) first source region and the (SS) second source region,

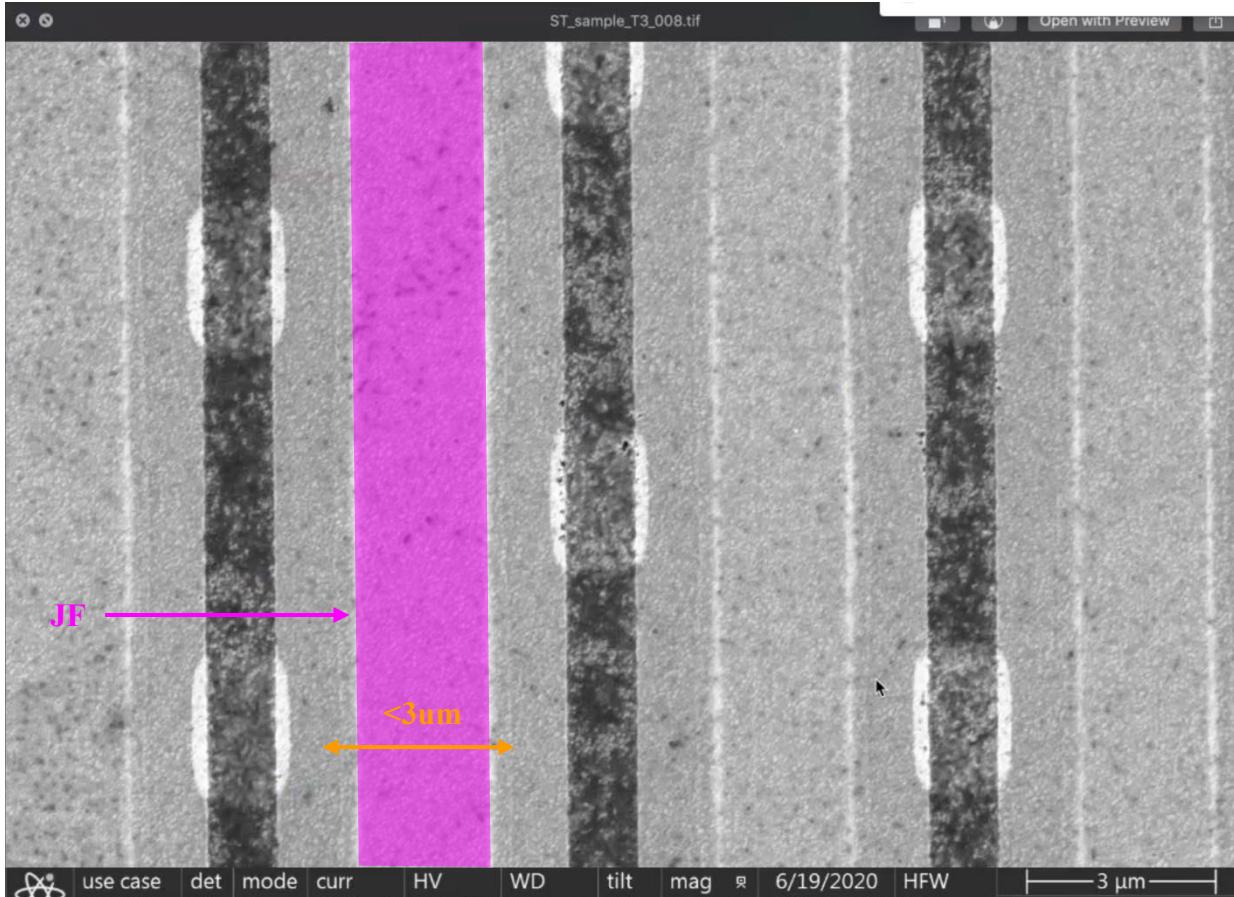


SEM SEPC



Claim 9

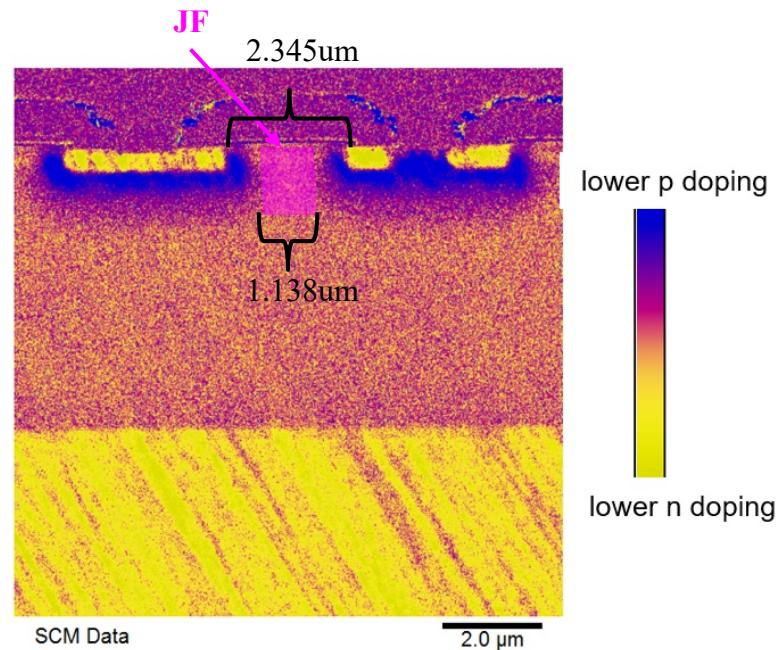
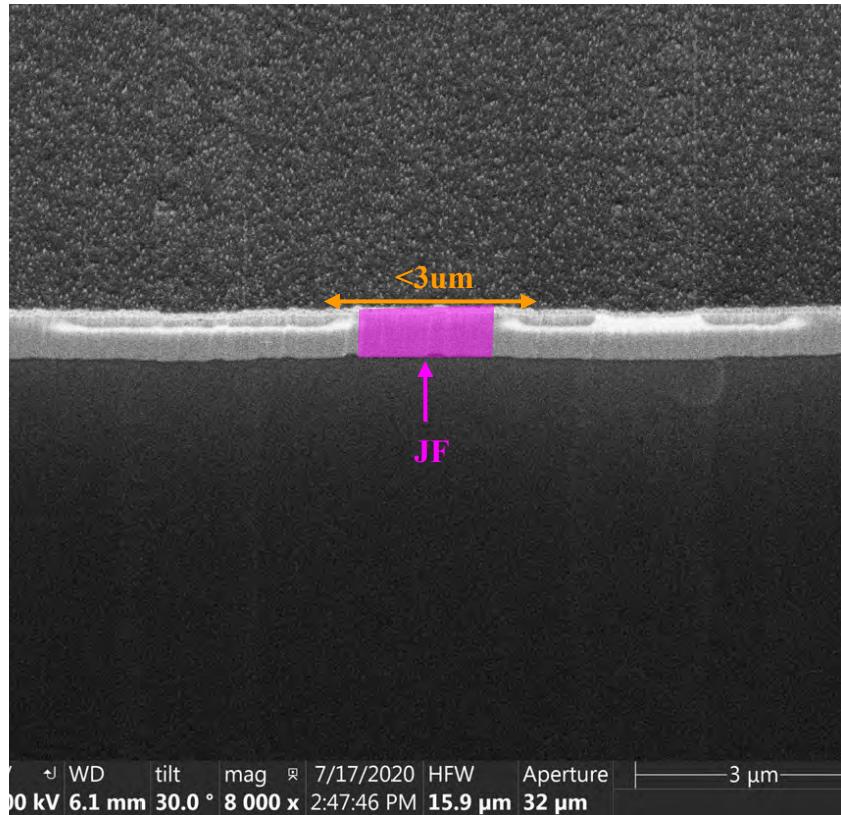
the (JF) JFET region having a width less than about three micrometers.



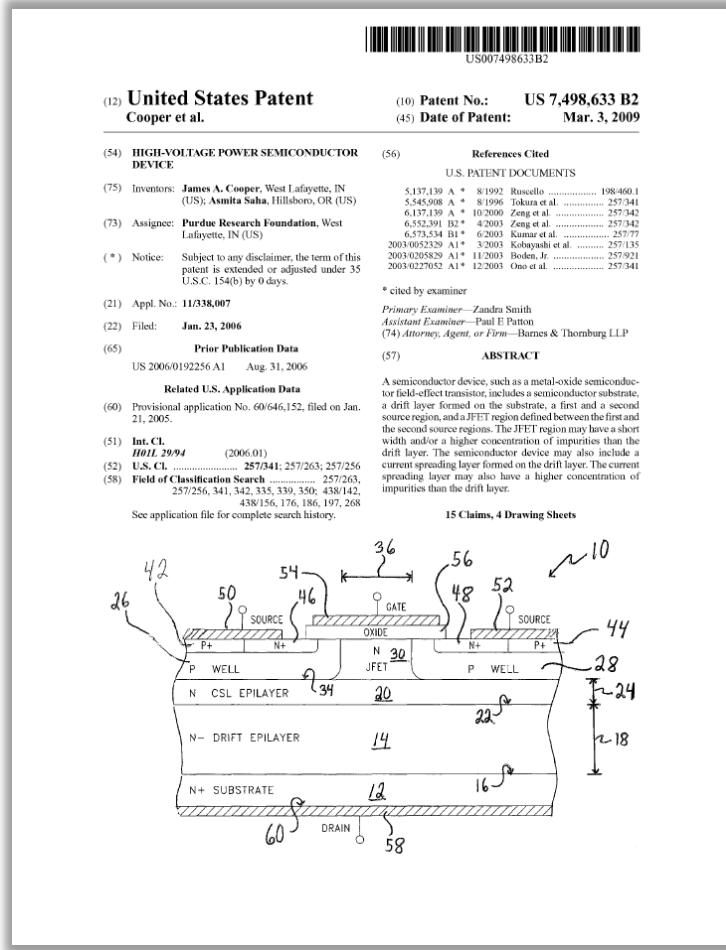
SEM SEPC

Claim 9

the (JF) JFET region having a width less than about three micrometers.



Note: SEM SEPC taken at B-B' cross section



**Title: HIGH-VOLTAGE POWER SEMICONDUCTOR DEVICE**

**Priority Date: Jan. 21, 2005**

**Filed Date: Jan. 23, 2006**

**Issued Date: Mar. 03, 2009**

**Expiration Date: Jan. 23, 2026**

**Inventors: James A. Cooper; Asmita Saha**

**Exemplary Claim: 9**

### Claim 9

A **double-implanted metal-oxide semiconductor field-effect transistor** comprising:

- a **(SUB) silicon-carbide substrate**;
- a **(DL) drift semiconductor layer** formed on a **(FS) front side** of the **(SUB) semiconductor substrate**;
- a **(FS) first source region**;
- a **(FSE) first source electrode** formed over the **(FS) first source region**, the **(FSE) first source electrode defining a longitudinal axis**;
- a **(FBC) plurality of first base contact regions** defined in the **(FS) first source region**,  
**(FBC) each of the plurality of first base contact regions being spaced apart from each other** in a **(FSE) direction parallel to the longitudinal axis defined by the first source electrode**;
- a **(SS) second source region**;
- a **(SSE) second source electrode** formed over the **(SS) second source region**, the **(SSE) second source electrode defining a longitudinal axis**;
- a **(SBC) plurality of second base contact regions** defined in the **(SS) second source region**,  
**(SBC) each of the plurality of second base contact regions being spaced apart from each other** in a **(SSE) direction parallel to the longitudinal axis defined by the second source electrode**; and
- a **(JF) JFET region** defined between the **(FS) first source region** and the **(SS) second source region**,  
**the (JF) JFET region having a width less than about three micrometers**.

Claim 9

A double-implanted metal-oxide semiconductor field-effect transistor comprising:

**SCTW70N120G2V**  
Datasheet

Silicon carbide Power MOSFET 1200 V, 91 A, 21 mΩ (typ.,  $T_J = 25^\circ\text{C}$ )  
in an HiP247 package

**Features**

Order code	$V_{DS}$	$R_{DS(on)} \text{ typ.}$	$I_D$
SCTW70N120G2V	1200 V	21 mΩ	91 A

- Very high operating junction temperature capability ( $T_J = 200^\circ\text{C}$ )
- Very fast and robust intrinsic body diode
- Extremely low gate charge and input capacitances

**Applications**

- Charger
- Power supply for renewable energy systems
- High frequency DC-DC converters

**Description**

This silicon carbide Power MOSFET is produced exploiting the advanced, innovative properties of wide bandgap materials. This results in unsurpassed on-resistance per unit area and very good switching performance almost independent of temperature. The outstanding thermal properties of the SiC material allow designers to use an industry-standard outline with significantly improved thermal capability. These features render the device perfectly suitable for high-efficiency and high power density applications.

HiP247

D(2, TAB)

G(1)

S(3)

AM0147sv1\_noZen

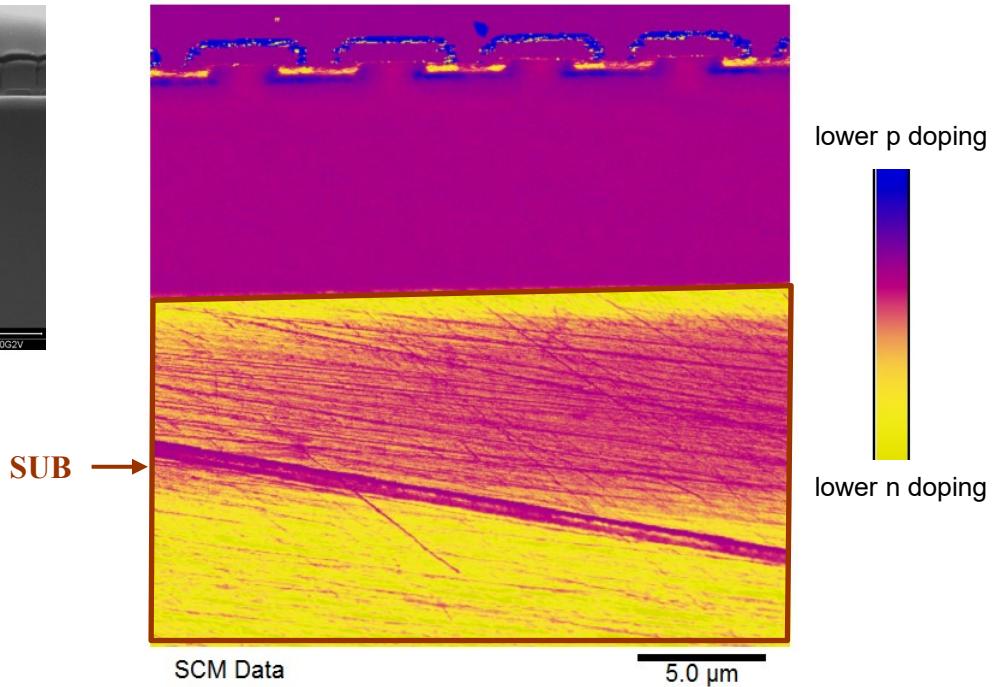
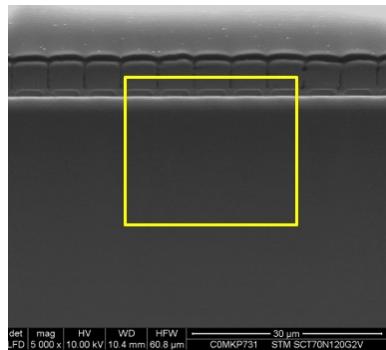
Claim 9

A double-implanted metal-oxide semiconductor field-effect transistor comprising:



Claim 9

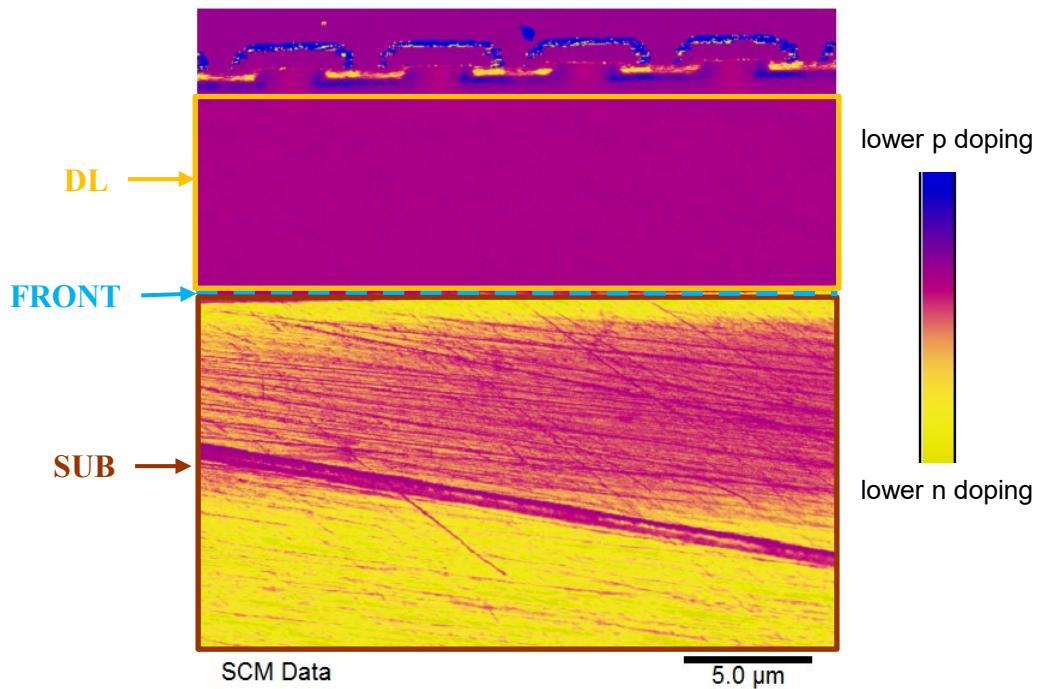
a (SUB) silicon-carbide substrate;



**Note:** Scanning Capacitance Microscopy (SCM) taken of the framed area in the Scanning Electron Microscopy (SEM) image

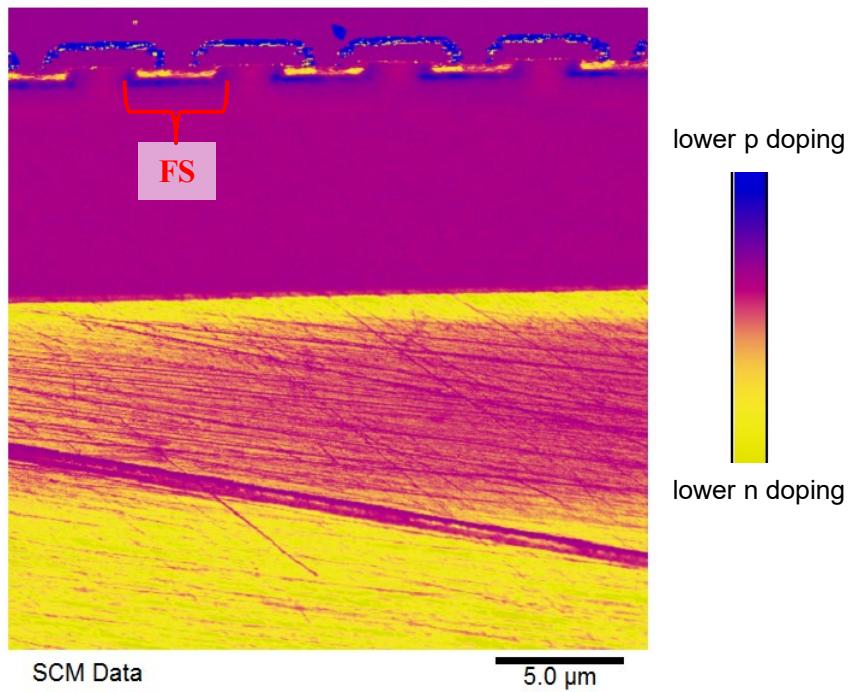
Claim 9

a (DL) drift semiconductor layer formed on a (FRONT) front side of the (SUB) semiconductor substrate;



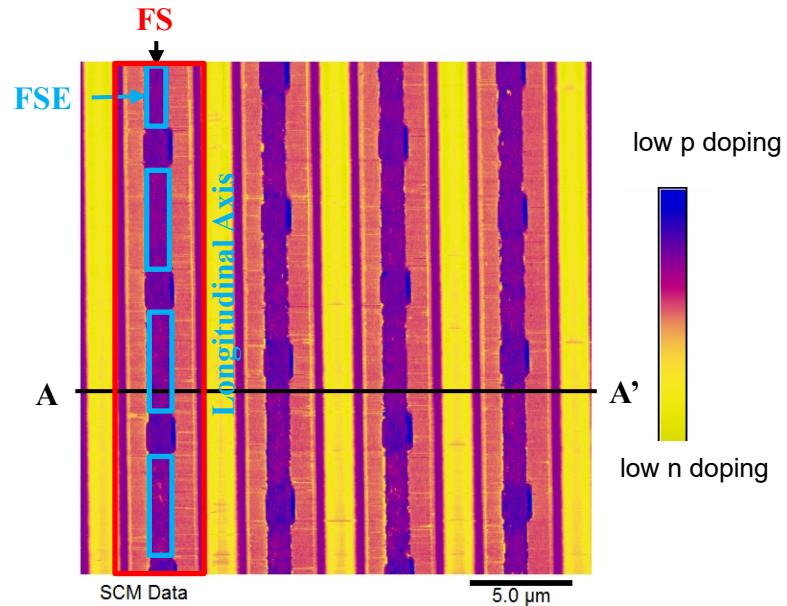
Claim 9

a (FS) first source region;

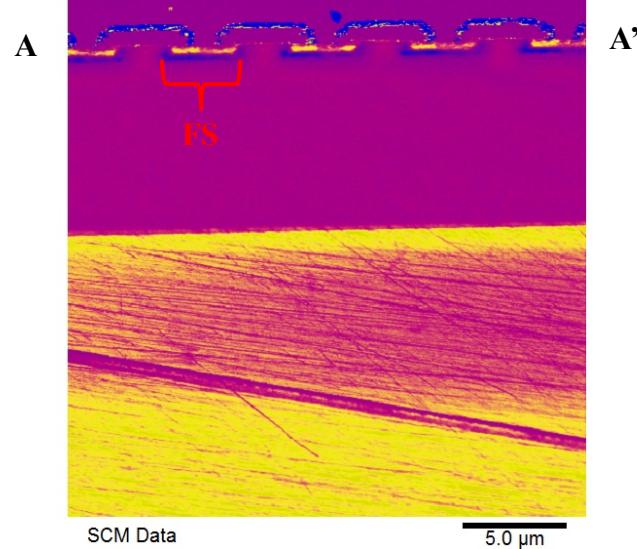


Claim 9

a (FSE) first source electrode formed over the (FS) first source region, the (FSE) first source electrode defining a longitudinal axis;



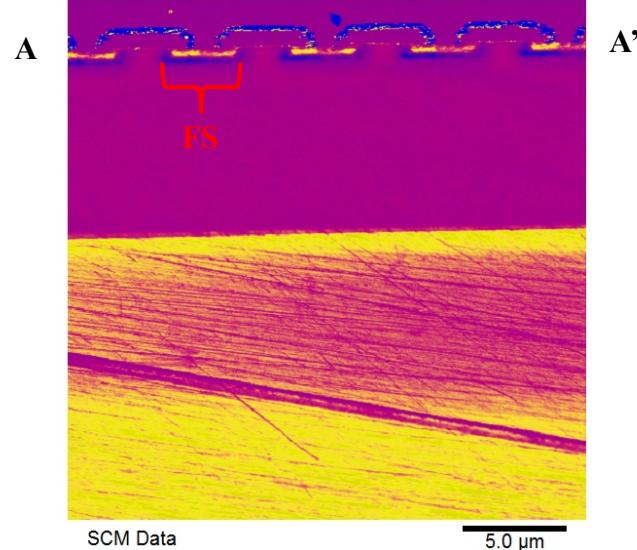
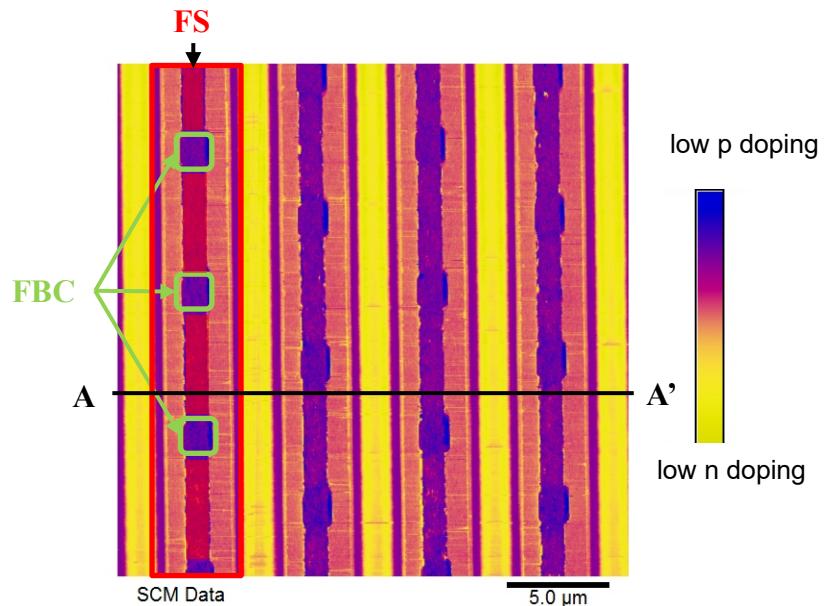
**Note:** Top view using SCM, after polishing down to the silicon carbide.



**Note:** SCM view taken at the A-A' cross-section.

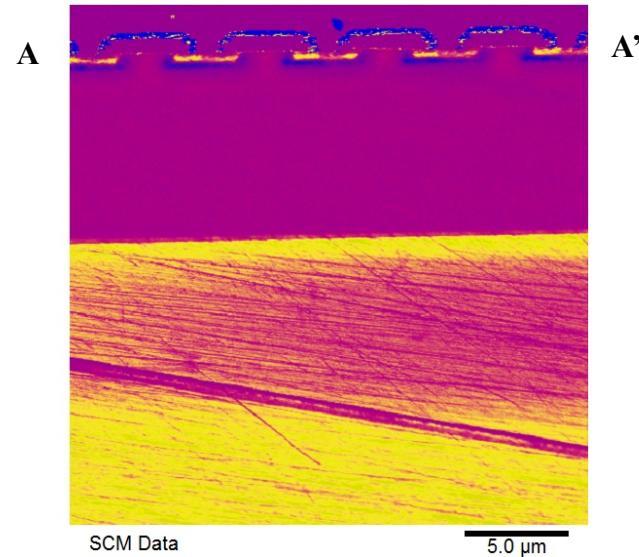
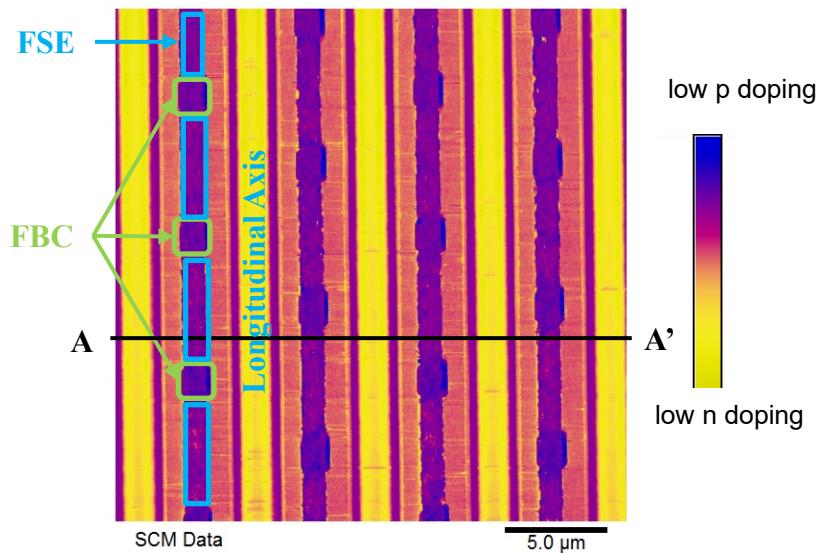
Claim 9

a (FBC) plurality of first base contact regions defined in the (FS) first source region,



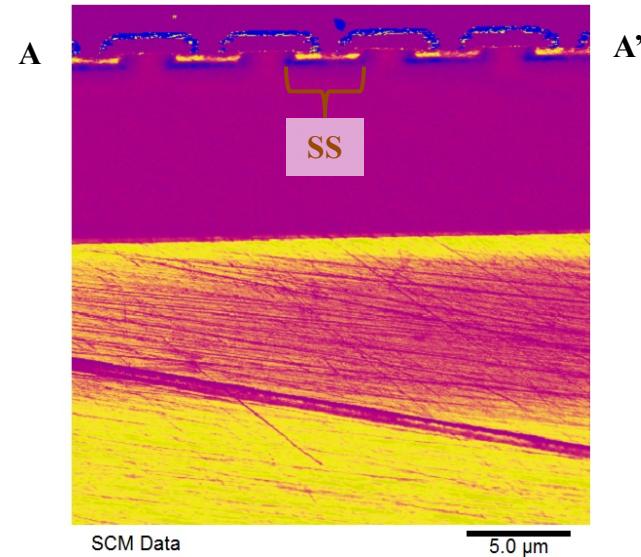
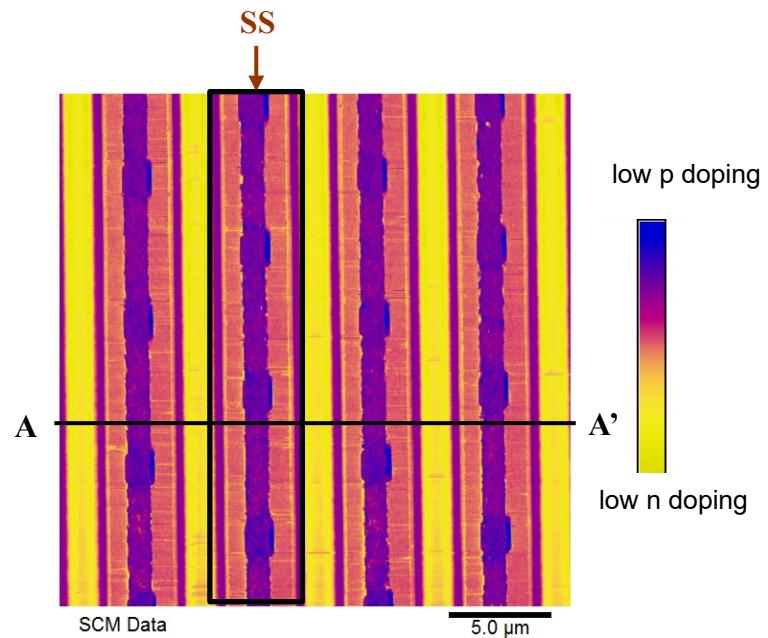
Claim 9

(FBC) each of the plurality of first base contact regions being spaced apart from each other in a (FSE) direction parallel to the longitudinal axis defined by the first source electrode;



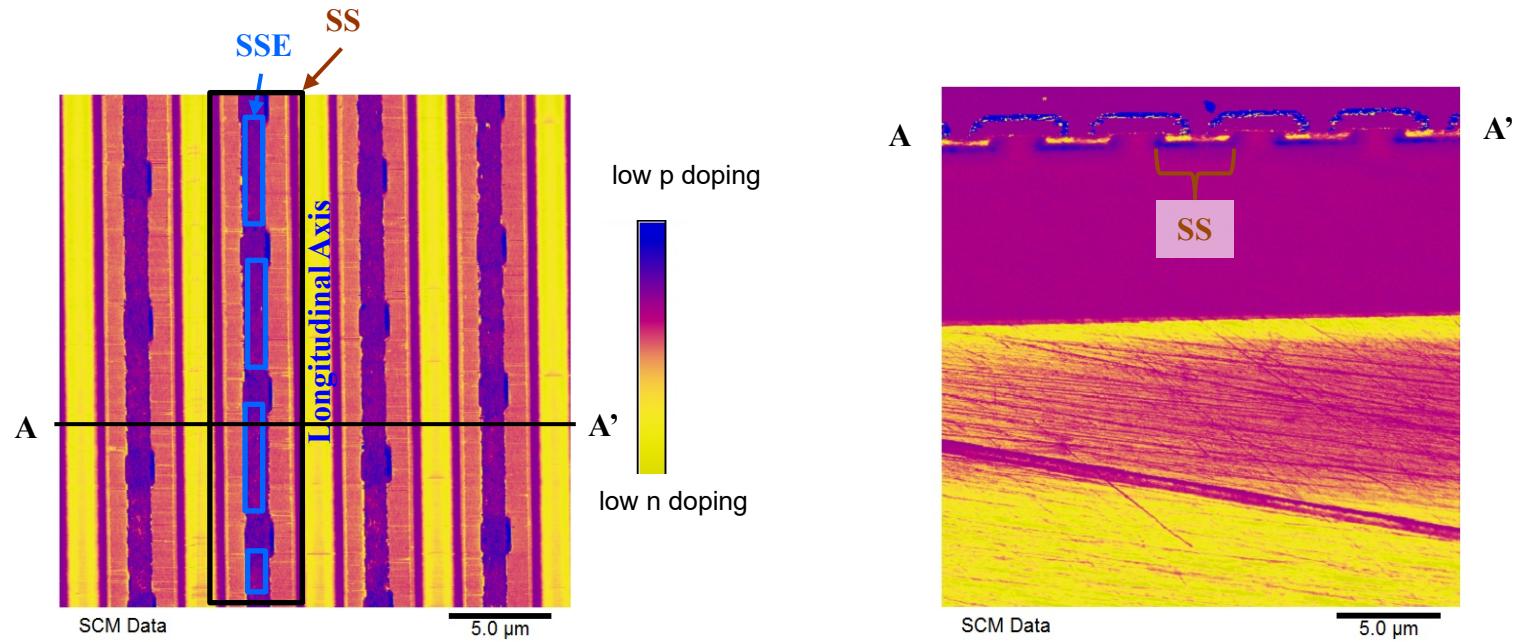
Claim 9

a (SS) second source region;



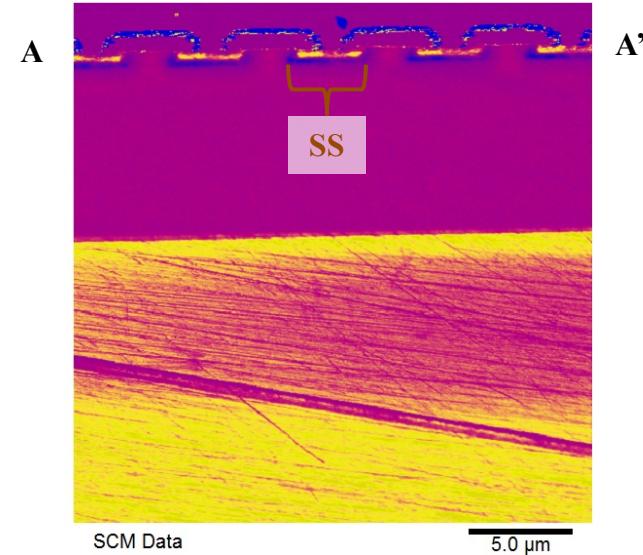
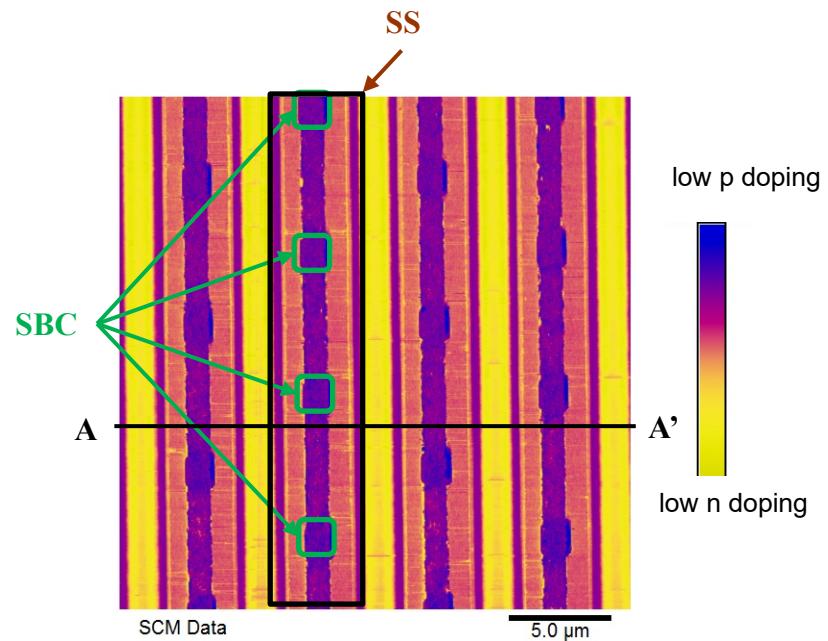
Claim 9

a (SSE) second source electrode formed over the (SS) second source region, the (SSE) second source electrode defining a longitudinal axis;



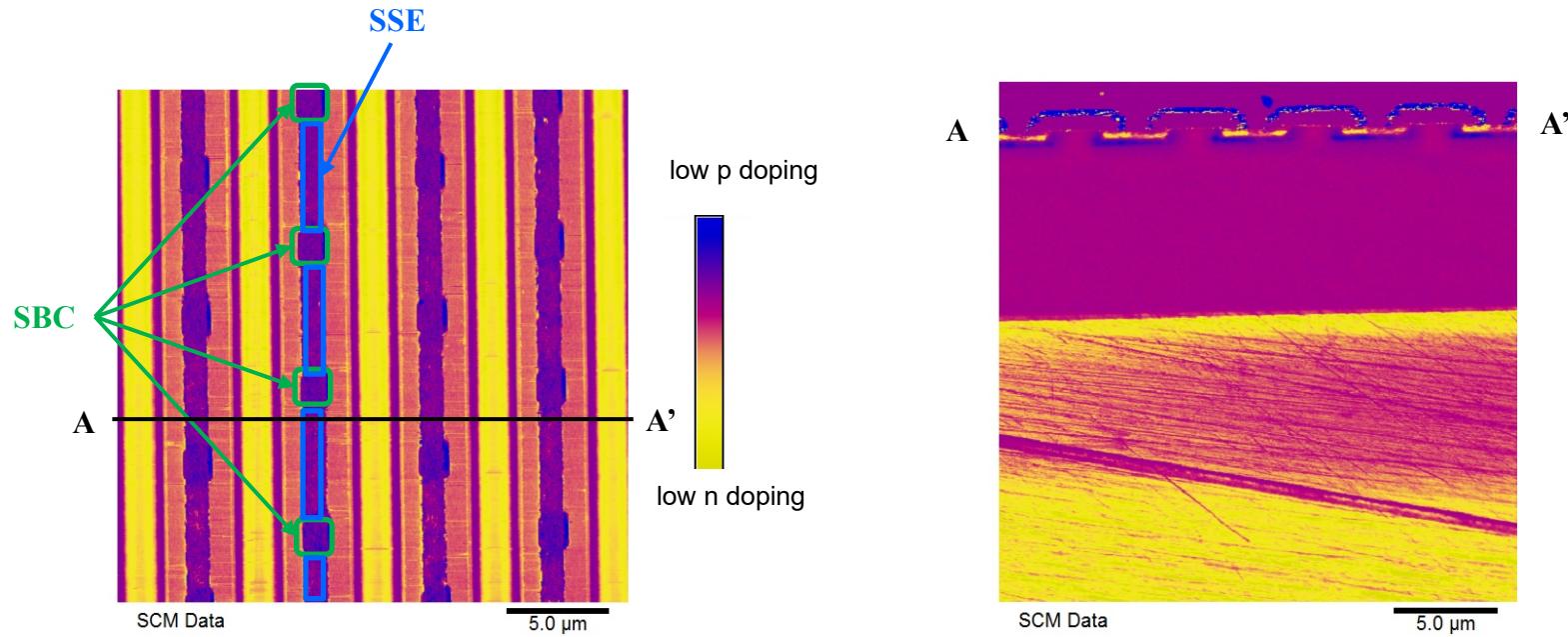
Claim 9

a (SBC) plurality of second base contact regions defined in the (SS) second source region,



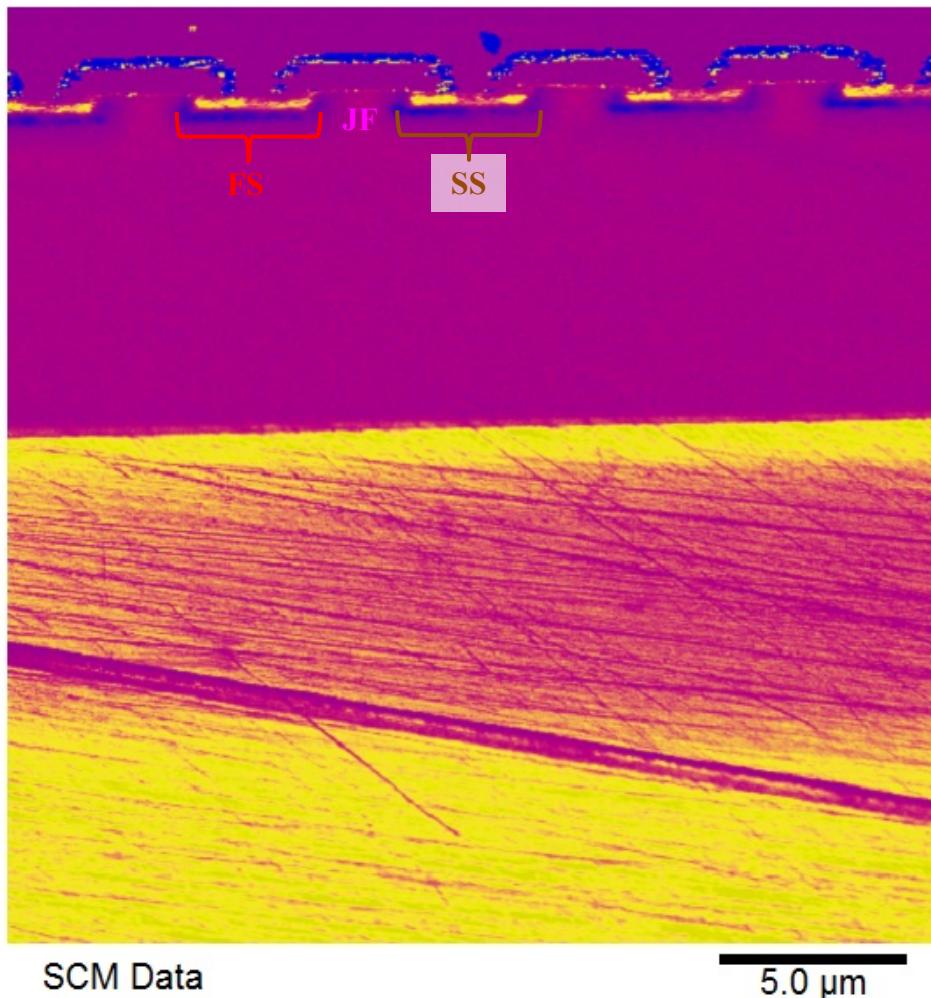
Claim 9

(SBC) each of the plurality of second base contact regions being spaced apart from each other in a (SSE) direction parallel to the longitudinal axis defined by the second source electrode; and



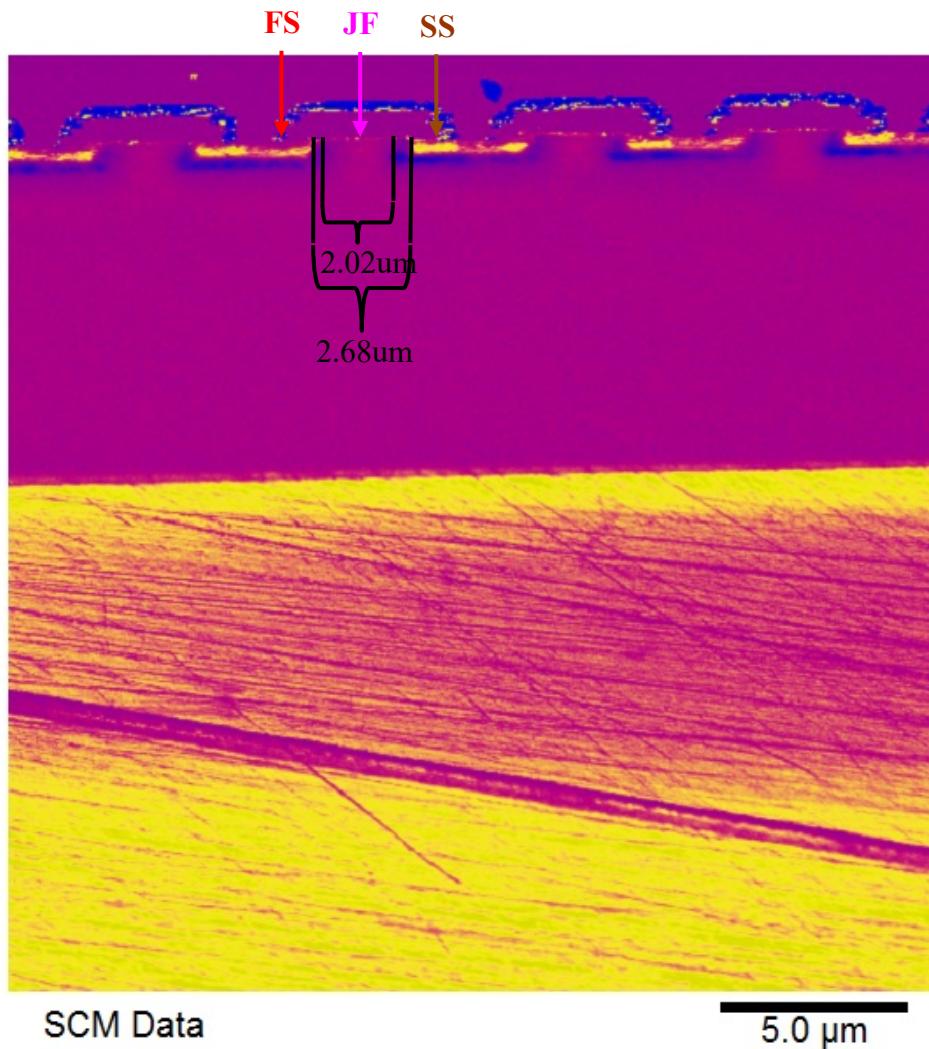
Claim 9

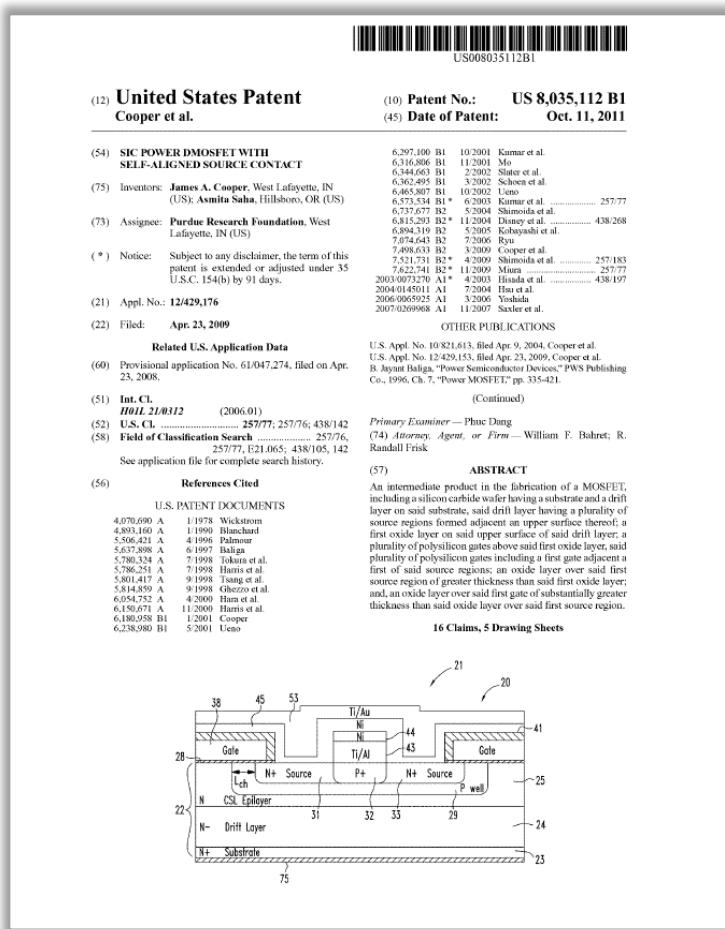
a (JF) JFET region defined between the (FS) first source region and the (SS) second source region,



Claim 9

the (JF) JFET region having a width less than about three micrometers.





# Title: SIC POWER DMOSFET WITH SELF-ALIGNED SOURCE CONTACT

## **Priority Date:** April 23, 2008

**Filed Date:** April 23, 2009

**Issued Date:** October 11, 2011

**Expiration Date:** July 23, 2029

**Inventors:** James A. Cooper; Asmita Saha

## **Exemplary Claim: 1**

**Claim 1**

A **silicon carbide power MOSFET**, comprising:

a **(SUB) silicon carbide wafer having a substrate** and a **(DFT) drift layer** on said **substrate**,  
said **(DFT) drift layer** having a **(SR) plurality of source regions formed adjacent** an **(US) upper surface**  
thereof;  
a **(GAT) plurality of polysilicon gates above** said **(DFT) drift layer**,  
said **(GAT) plurality of polysilicon gates** including a **(GAT1) first gate** adjacent a **(SR1) first of said source**  
**regions**,  
said **(GAT1) first gate** having a **(TOP) top surface**, a **(BOT) lower surface** and a **(SW) sidewall**,  
said **(SW) sidewall overlying** said **(SR1) first source region**;  
a **(SOX) first oxide layer between** said **(BOT) first gate lower surface** and said **(US) upper surface** of said  
**(DFT) drift layer**;  
a **(ILD) second, thicker oxide layer** over said **(TOP) top surface** and **(SW) sidewall** of said **(GAT1) first gate**;  
and  
a **(ML) conformal layer of metal** extending laterally across said **(GAT1) first gate (TOP) top surface** and  
**(SW) sidewall** and said **adjacent (SR1) first source region**.

Claim 1

A silicon carbide power MOSFET, comprising:

**SCTW90N65G2V**

Datasheet

Silicon carbide Power MOSFET 650 V, 119 A, 18 mΩ (typ.,  $T_J = 25^\circ\text{C}$ ) in an HiP247 package

**Features**

Order code	$V_{DS}$	$R_{DS(on)} \text{ max.}$	$I_D$
SCTW90N65G2V	650 V	24 mΩ	119 A

- Very high operating junction temperature capability ( $T_J = 200^\circ\text{C}$ )
- Very fast and robust intrinsic body diode
- Extremely low gate charge and input capacitances

**HIP247**

**Circuit Diagram**

**Applications**

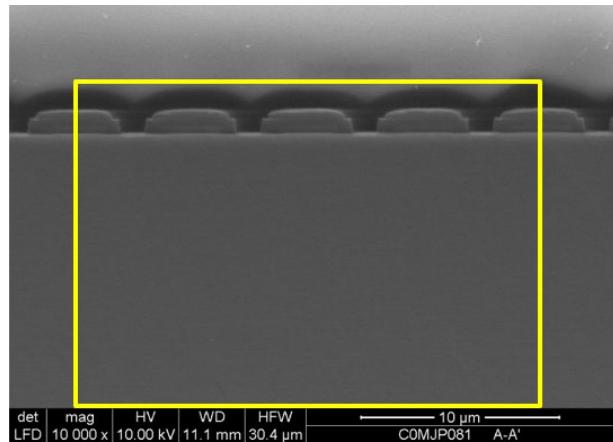
- Switching applications
- Power supply for renewable energy systems
- High frequency DC-DC converters

**Description**

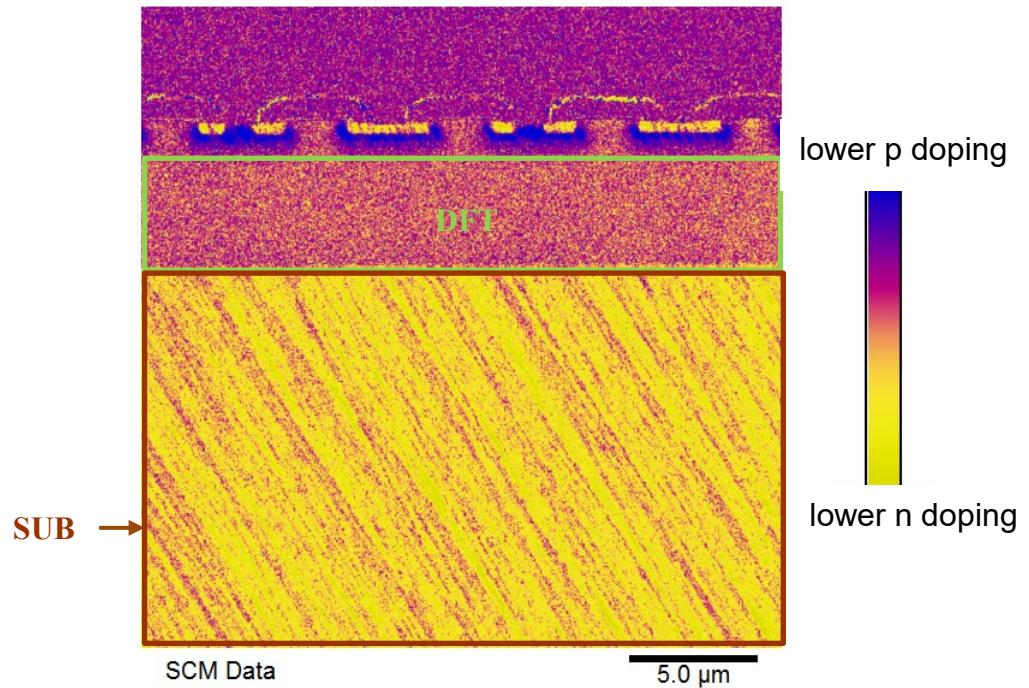
This silicon carbide Power MOSFET device has been developed using ST's advanced and innovative 2<sup>nd</sup> generation SiC MOSFET technology. The device features remarkably low on-resistance per unit area and very good switching performance. The variation of switching loss is almost independent of junction temperature.

Claim 1

a (SUB) silicon carbide wafer having a substrate and a (DFT) drift layer on said substrate,



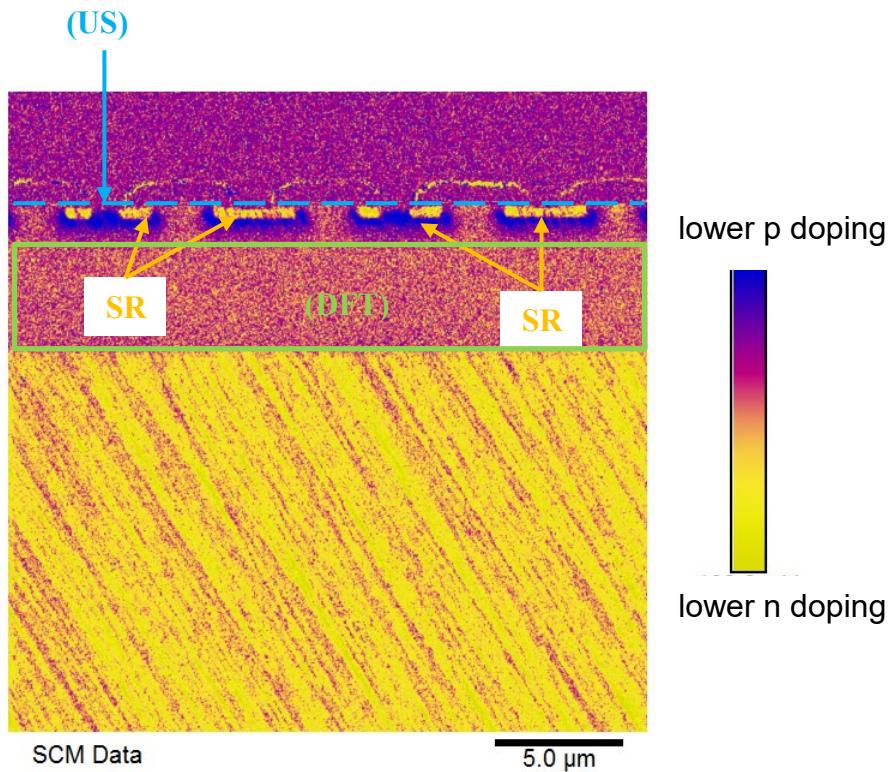
SEM



**Note:** Scanning Capacitance Microscopy (SCM) of the framed area in the Scanning Electron Microscopy (SEM) image.

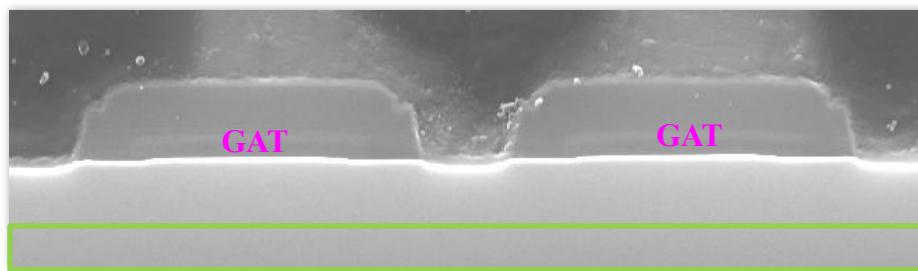
Claim 1

said **(DFT) drift layer** having a **(SR) plurality of source regions** formed adjacent an **(US) upper surface** thereof;

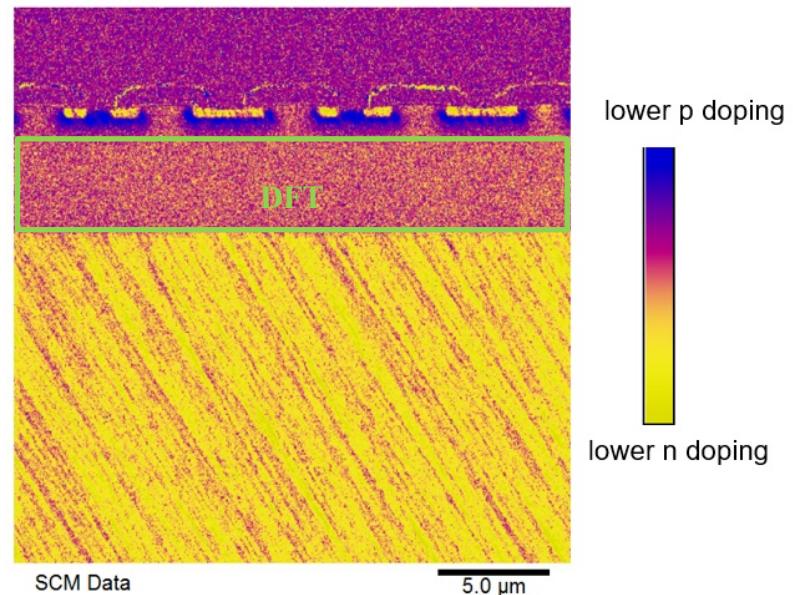


Claim 1

a (GAT) plurality of polysilicon gates above said (DFT) drift layer,

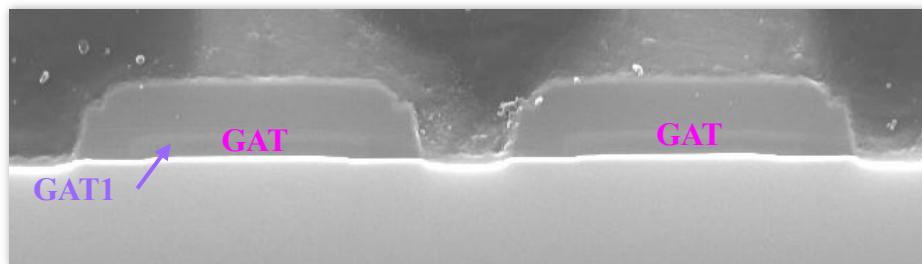


DFT  
SEM

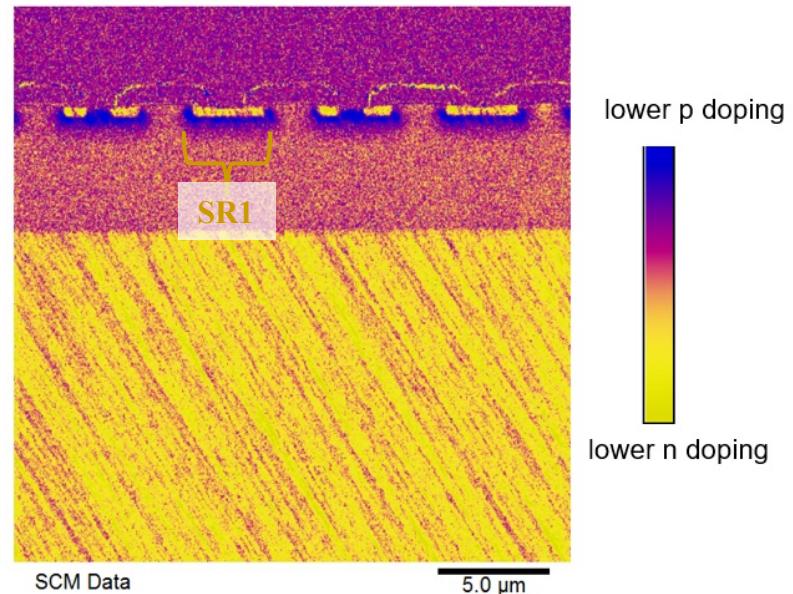


Claim 1

said **(GAT)** plurality of polysilicon gates including a **(GAT1)** first gate adjacent a **(SR1)** first of said source regions,

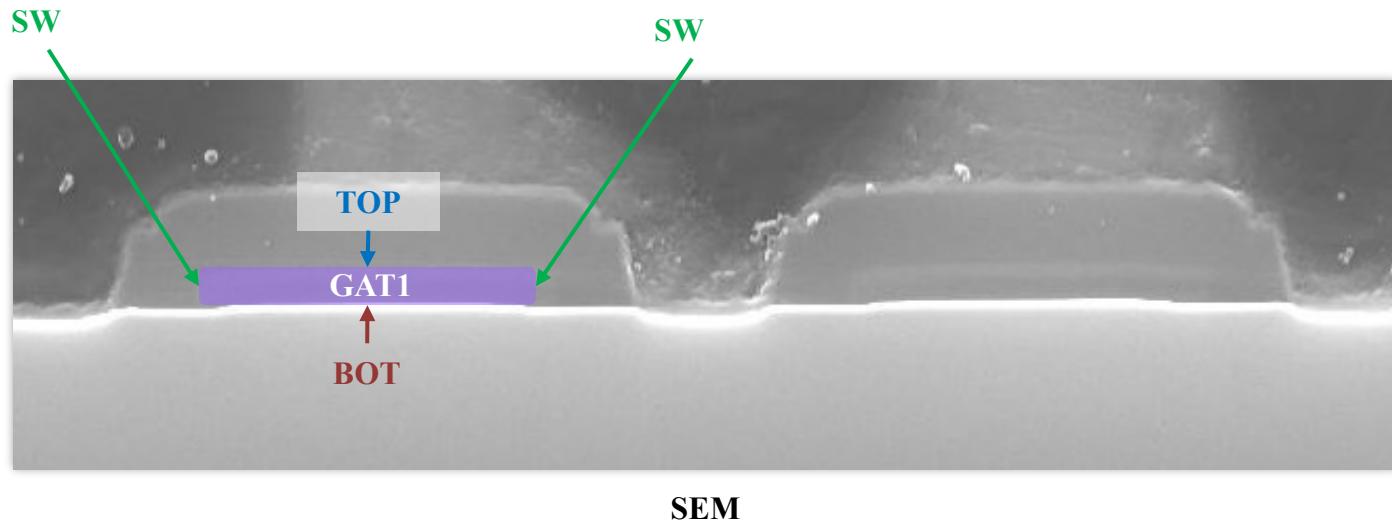


SEM



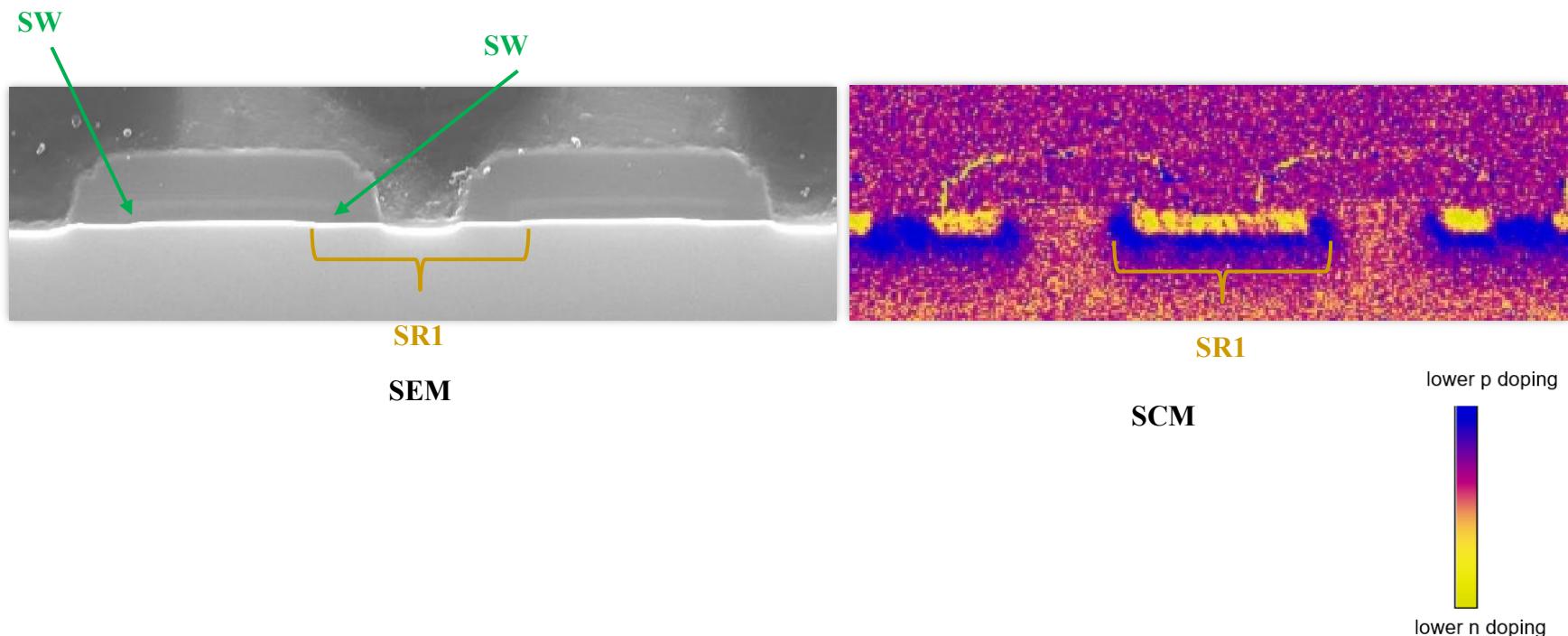
Claim 1

said (GAT1) first gate having a (TOP) top surface, a (BOT) lower surface and a (SW) sidewall,



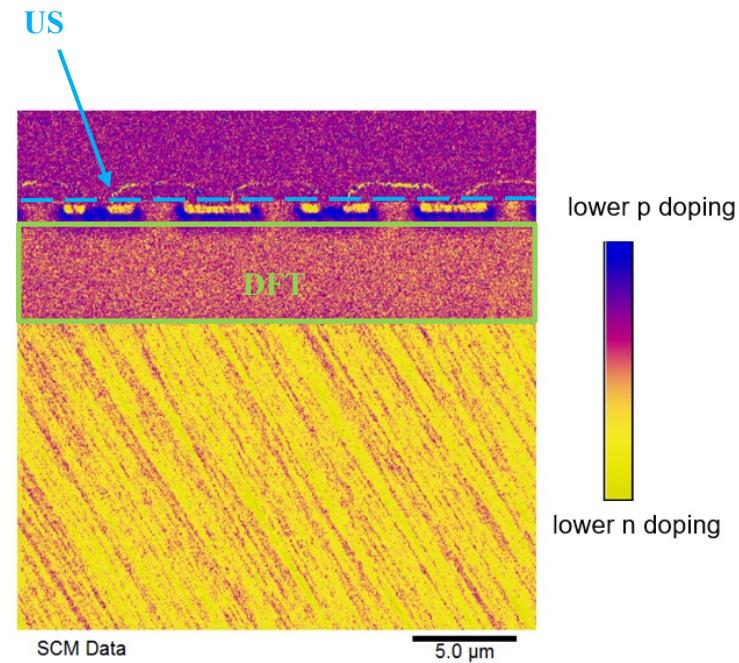
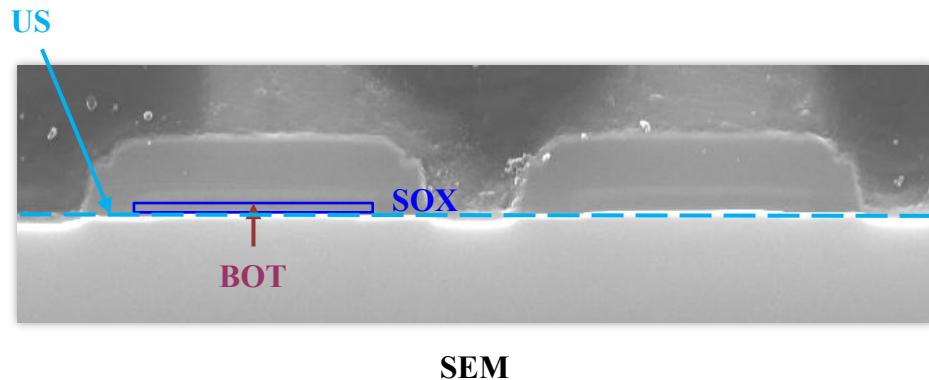
Claim 1

said (SW) sidewall overlying said (SR1) first source region;



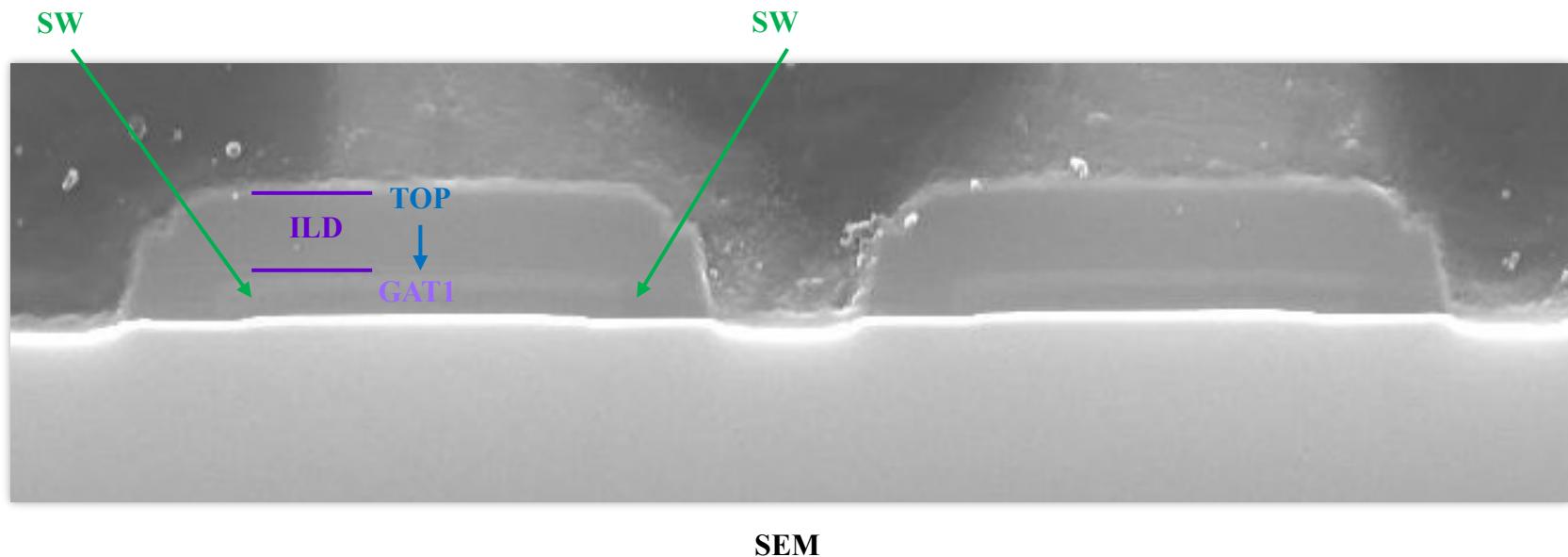
Claim 1

a (SOX) first oxide layer between said (BOT) first gate lower surface and said (US) upper surface of said (DFT) drift layer;



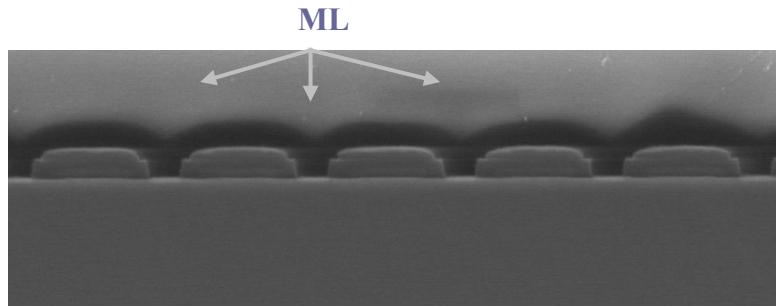
Claim 1

a (ILD) second, thicker oxide layer over said (TOP) top surface and (SW) sidewall of said (GAT1) first gate; and

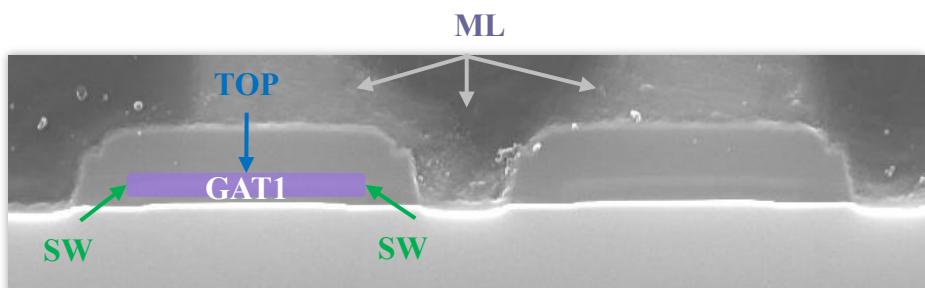


Claim 1

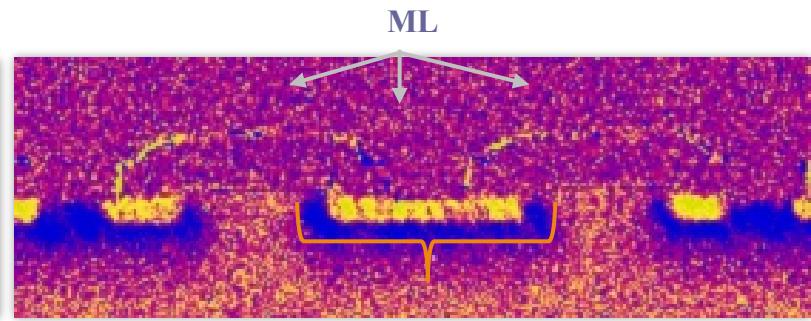
a (ML) conformal layer of metal extending laterally across said (GAT1) first gate (TOP) top surface and (SW) sidewall and said adjacent (SR1) first source region.



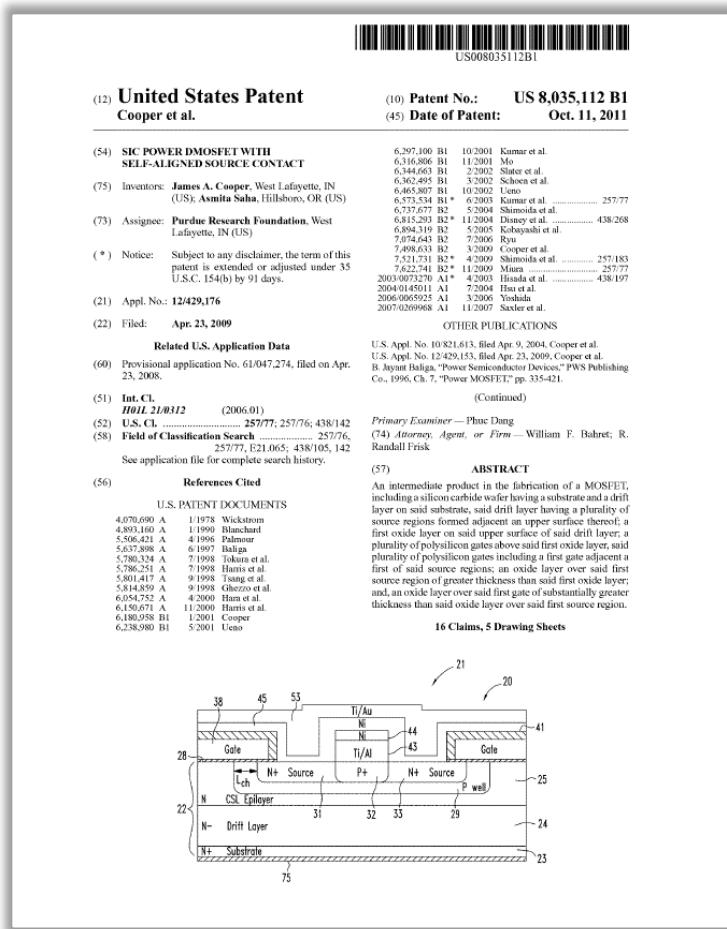
SEM



SEM



SCM



**Title: SIC POWER DMOSFET WITH SELF-ALIGNED SOURCE CONTACT**

**Priority Date:** April 23, 2008

**Filed Date:** April 23, 2009

**Issued Date:** October 11, 2011

**Expiration Date:** July 23, 2029

**Inventors:** James A. Cooper; Asmita Saha

**Exemplary Claim:** 1

**Claim 1**

A **silicon carbide power MOSFET**, comprising:

a **(SUB) silicon carbide wafer having a substrate** and a **(DFT) drift layer** on said **substrate**,  
said **(DFT) drift layer** having a **(SR) plurality of source regions formed adjacent** an **(US) upper surface**  
thereof;  
a **(GAT) plurality of polysilicon gates above** said **(DFT) drift layer**,  
said **(GAT) plurality of polysilicon gates** including a **(GAT1) first gate** adjacent a **(SR1) first of said source**  
**regions**,  
said **(GAT1) first gate** having a **(TOP) top surface**, a **(BOT) lower surface** and a **(SW) sidewall**,  
said **(SW) sidewall overlying** said **(SR1) first source region**;  
a **(SOX) first oxide layer between** said **(BOT) first gate lower surface** and said **(US) upper surface** of said  
**(DFT) drift layer**;  
a **(ILD) second, thicker oxide layer** over said **(TOP) top surface** and **(SW) sidewall** of said **(GAT1) first gate**;  
and  
a **(ML) conformal layer of metal** extending laterally across said **(GAT1) first gate (TOP) top surface** and  
**(SW) sidewall** and said **adjacent (SR1) first source region**.

Claim 1

A silicon carbide power MOSFET, comprising:

**SCTW70N120G2V**  
Datasheet

Silicon carbide Power MOSFET 1200 V, 91 A, 21 mΩ (typ.,  $T_J = 25^\circ\text{C}$ )  
in an HiP247 package

**Features**

Order code	$V_{DS}$	$R_{DS(on)} \text{ typ.}$	$I_D$
SCTW70N120G2V	1200 V	21 mΩ	91 A

- Very high operating junction temperature capability ( $T_J = 200^\circ\text{C}$ )
- Very fast and robust intrinsic body diode
- Extremely low gate charge and input capacitances

**Applications**

- Charger
- Power supply for renewable energy systems
- High frequency DC-DC converters

**Description**

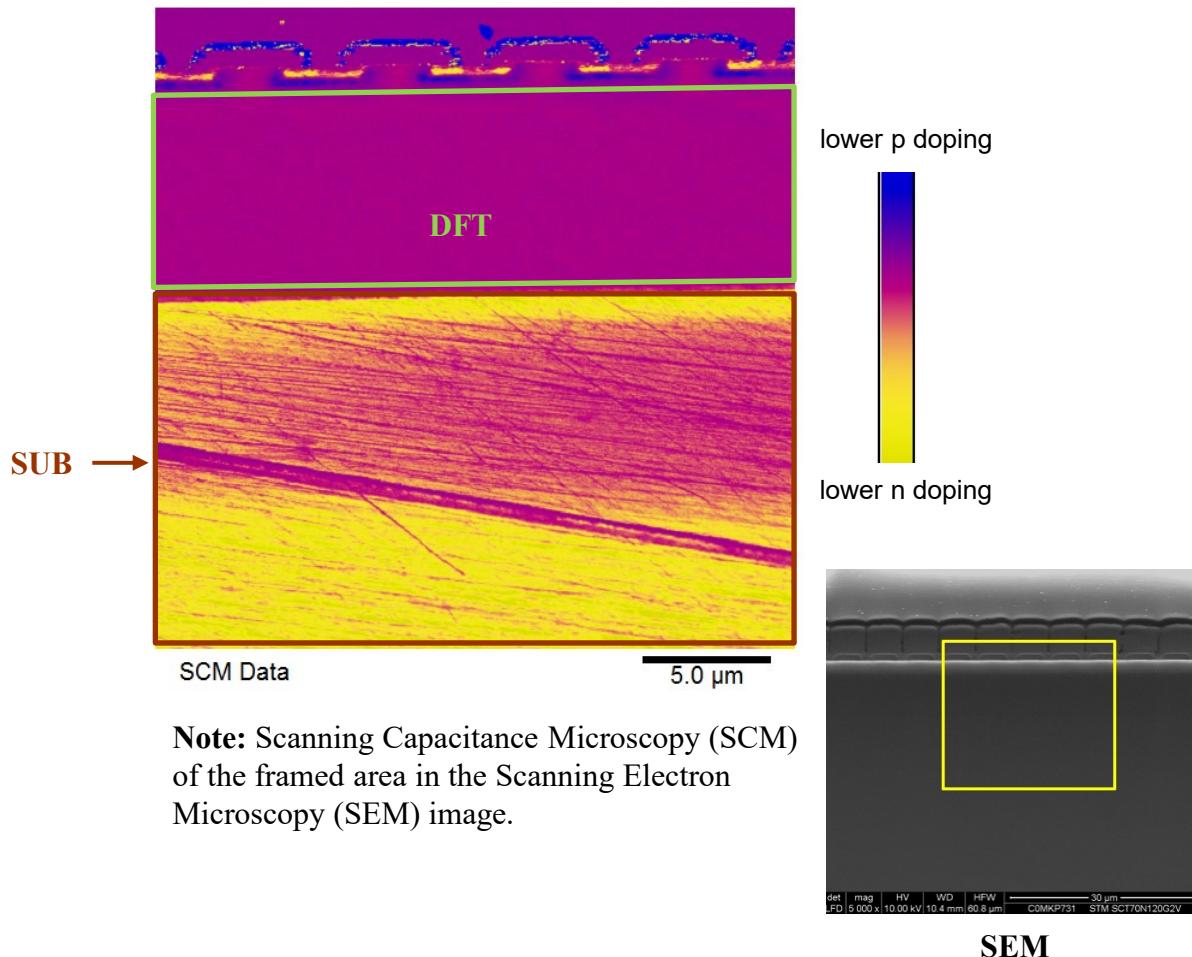
This silicon carbide Power MOSFET is produced exploiting the advanced, innovative properties of wide bandgap materials. This results in unsurpassed on-resistance per unit area and very good switching performance almost independent of temperature. The outstanding thermal properties of the SiC material allow designers to use an industry-standard outline with significantly improved thermal capability. These features render the device perfectly suitable for high-efficiency and high power density applications.

HiP247

AM0147sv1\_noZen

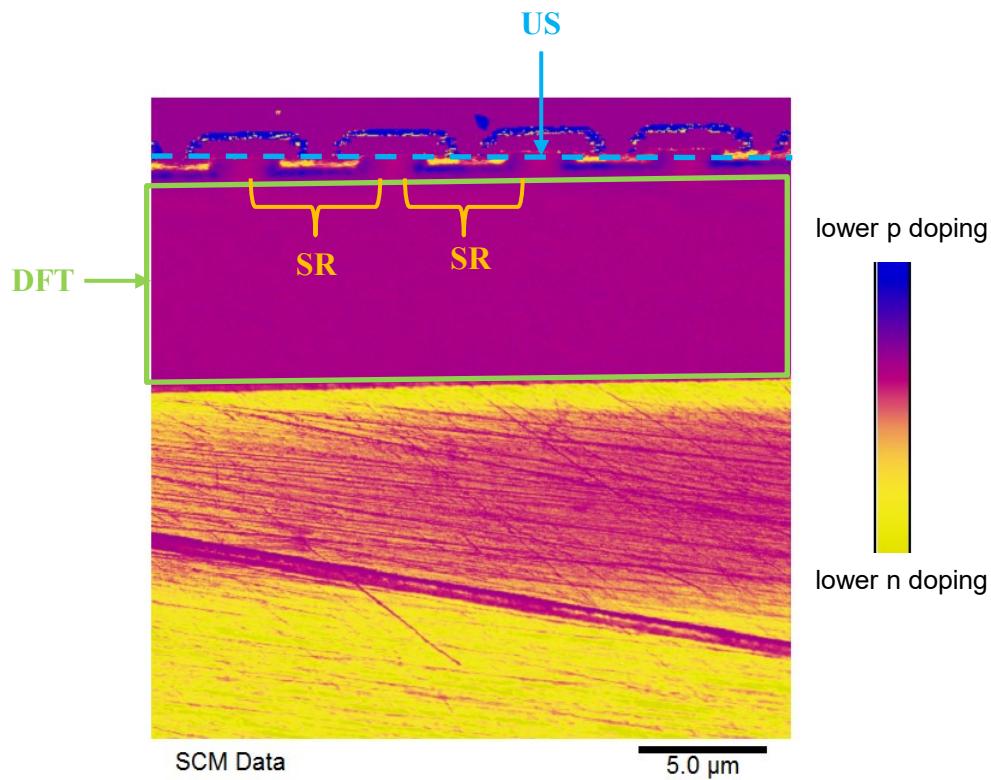
Claim 1

a (SUB) silicon carbide wafer having a substrate and a (DFT) drift layer on said substrate,



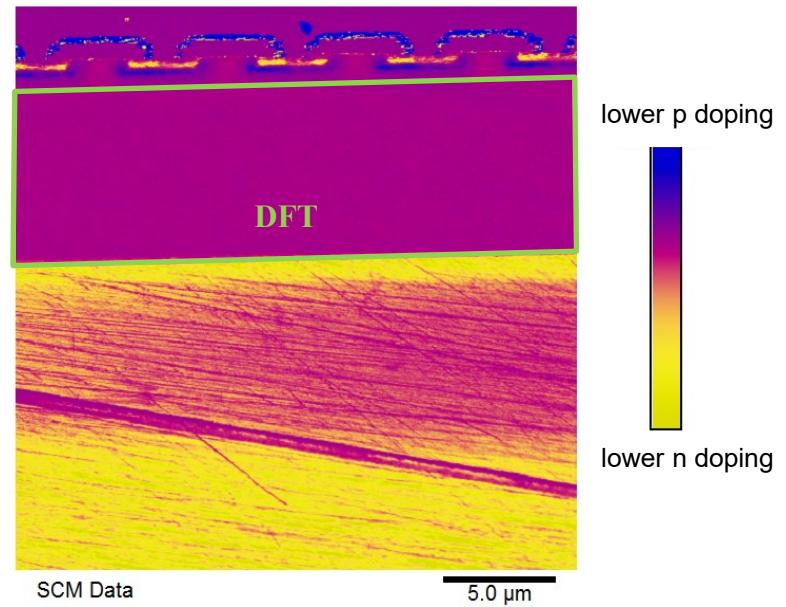
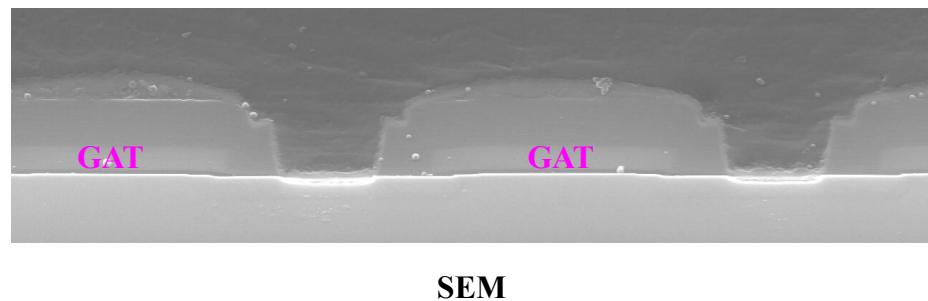
Claim 1

said **(DFT)** drift layer having a **(SR)** plurality of source regions formed adjacent an **(US)** upper surface thereof;



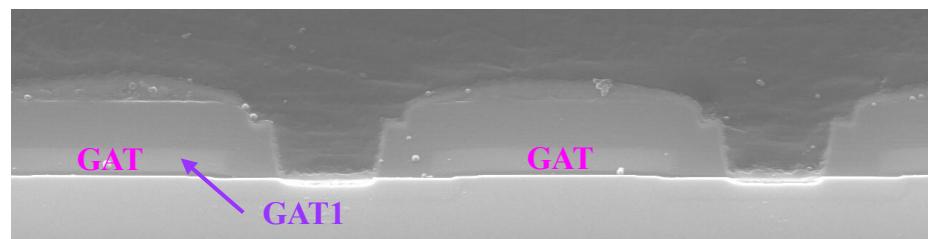
Claim 1

a (GAT) plurality of polysilicon gates above said (DFT) drift layer,

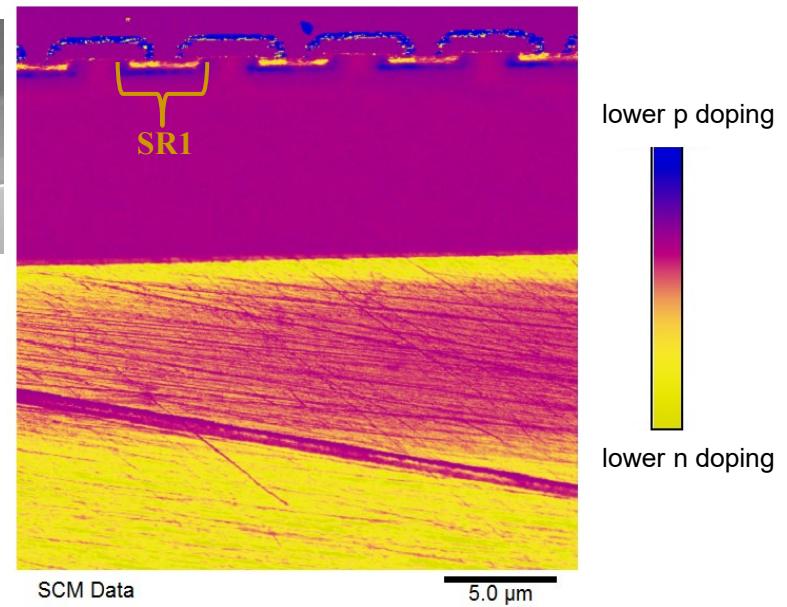


Claim 1

said (GAT) plurality of polysilicon gates including a (GAT1) first gate adjacent a (SR1) first of said source regions,

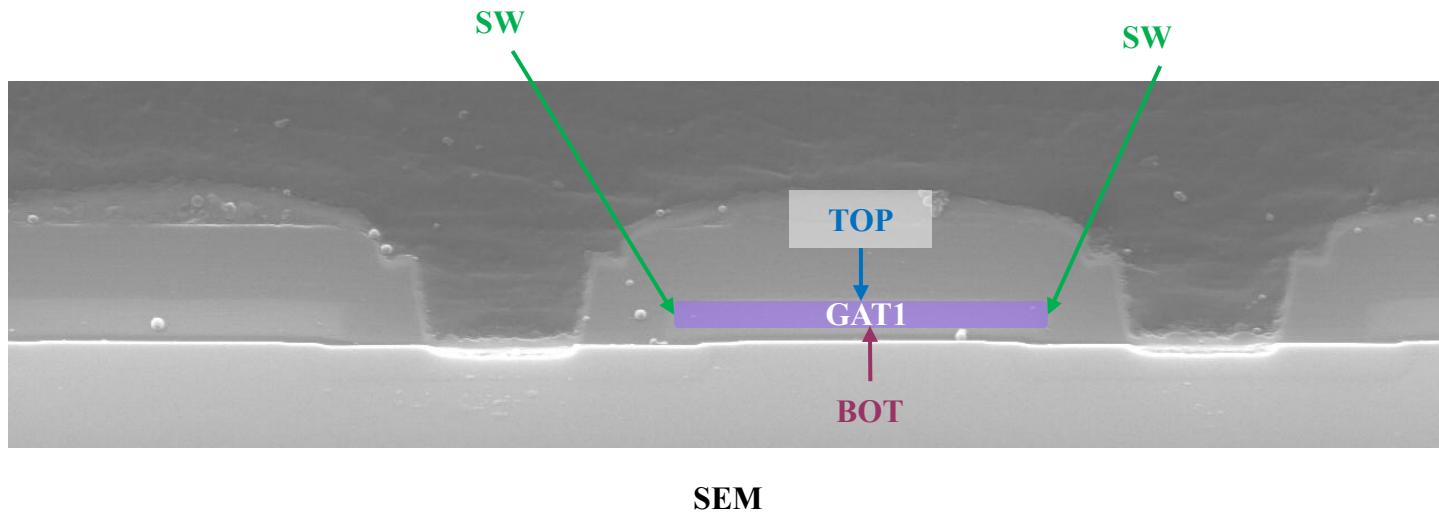


SEM



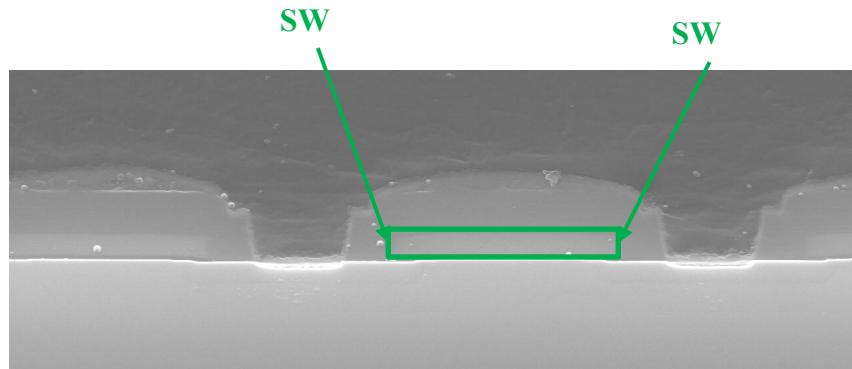
Claim 1

said (GAT1) first gate having a (TOP) top surface, a (BOT) lower surface and a (SW) sidewall,

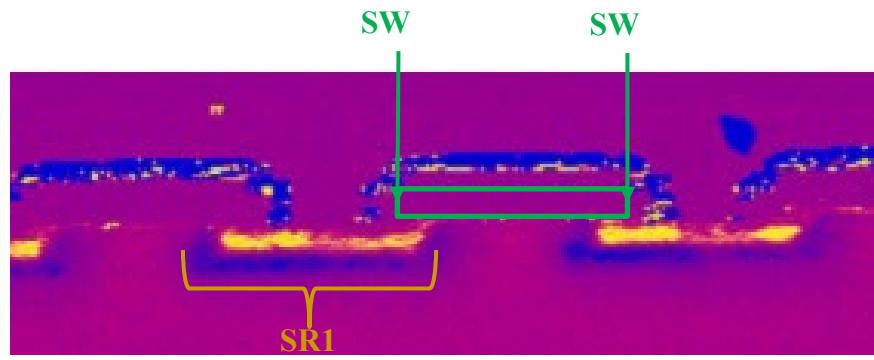


Claim 1

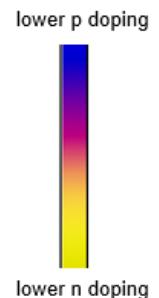
said (SW) sidewall overlying said (SR1) first source region;



SEM

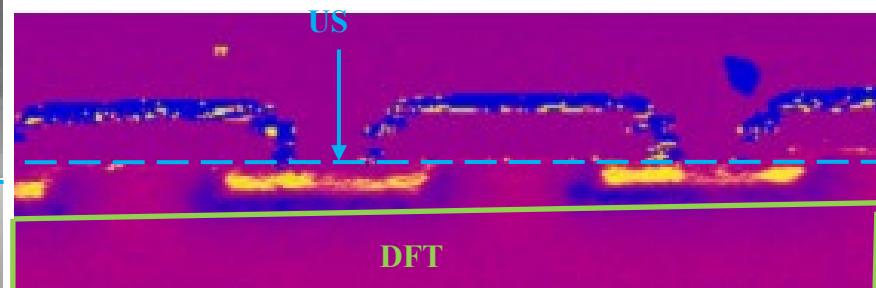
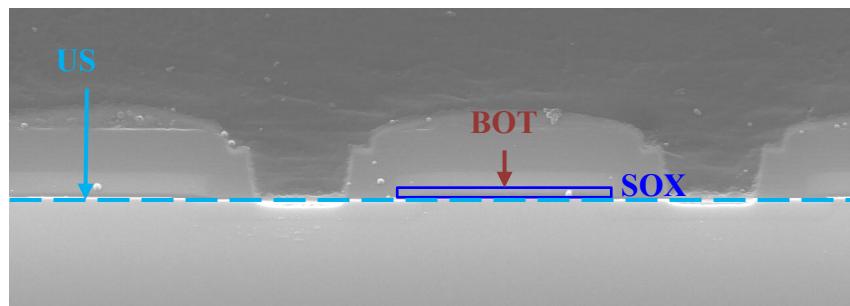


SCM



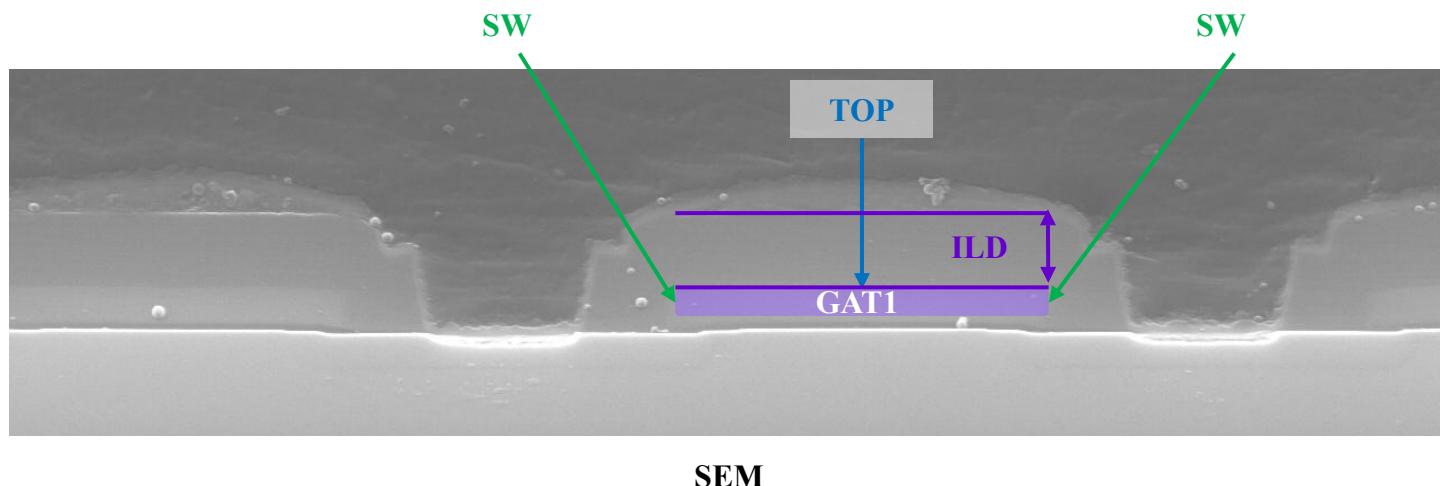
Claim 1

a (SOX) first oxide layer between said (BOT) first gate lower surface and said (US) upper surface of said (DFT) drift layer;



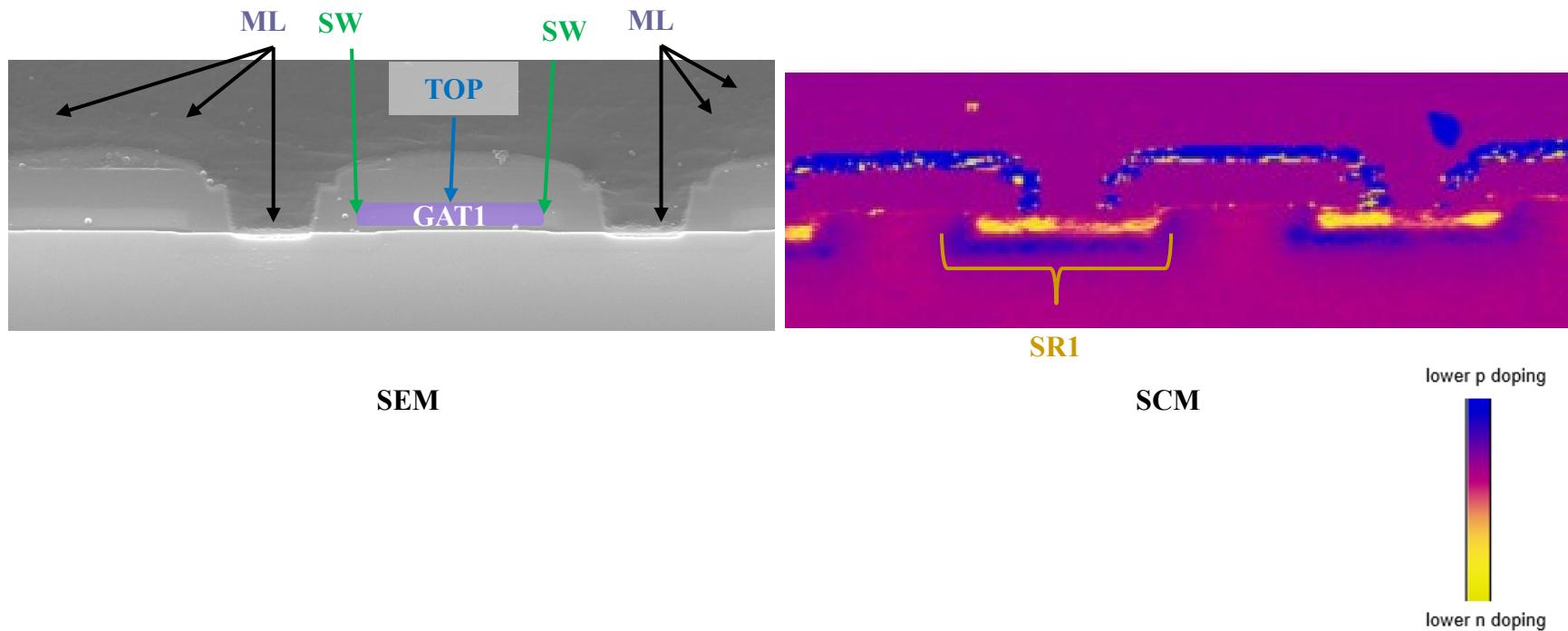
Claim 1

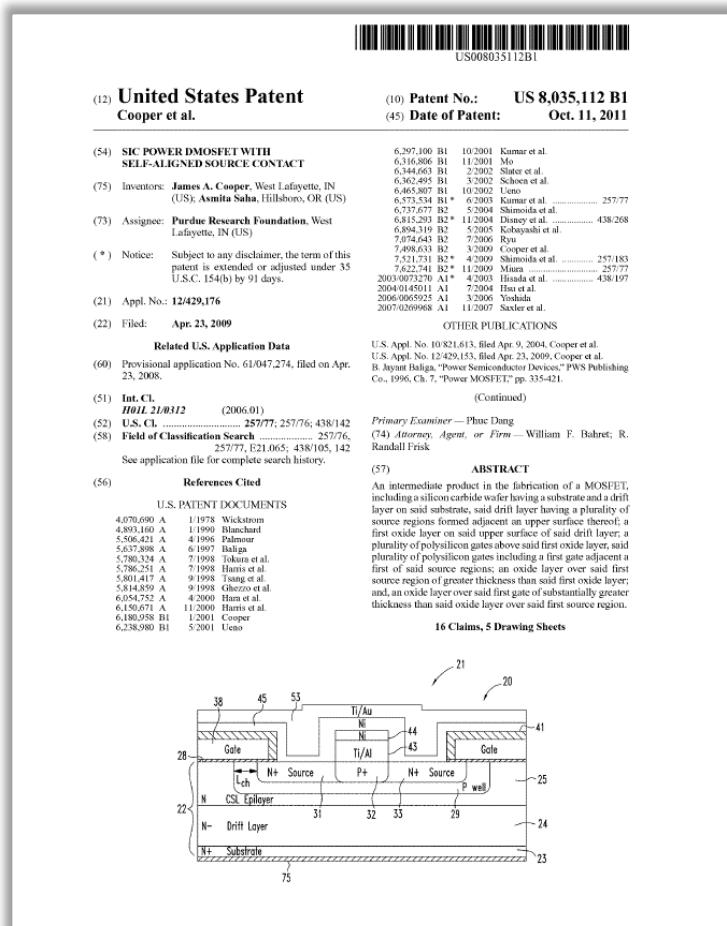
a (ILD) second, thicker oxide layer over said (TOP) top surface and (SW) sidewall of said (GAT1) first gate; and



Claim 1

a (ML) conformal layer of metal extending laterally across said (GAT1) first gate (TOP) top surface and (SW) sidewall and said adjacent (SR1) first source region.





**Title: SIC POWER DMOSFET WITH SELF-ALIGNED SOURCE CONTACT**

**Priority Date:** April 23, 2008

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**Expiration Date:** July 23, 2029

**Inventors:** James A. Cooper; Asmita Saha

**Exemplary Claims:** 6, 7, 10, 11, 12

### Claim 6

A **mosfet structure**, comprising:

a **(SUB) silicon carbide wafer having a substrate body** with an **(US) upper surface**,  
said **(SUB) substrate body** having **(SR) at least one source region** formed **(US) adjacent said upper surface**;  
a **(SOX) substrate surface oxidation layer** on said **(US) upper surface** of said **(SUB) substrate body** and **(SR) adjacent said source region**;

**(GAT) at least two polysilicon gates** above said **(SOX) substrate surface oxidation layer**, said **(GAT) gates** each having a **(TOP) top**, a **(BOT) bottom** and **(SID) sides**, wherein a **(SR) first source region** of said **at least one source region** is juxtaposed between **(GAT) first and second adjacent gates** of said **at least two polysilicon gates**;

a **(ILD) gate oxide layer**, thicker than said **(SOX) substrate surface oxidation layer**, over said **(TOP) tops** and **(SID) sides** of **(GAT) each of said gates**; and

a **(ML) material layer** over said **(SR) first source region** and between said **(ILD) gate oxide layers** on said **(SID) sides** of said **(GAT) gates**,

said **(ML) material layer** comprising one of an oxide and a **(ML) metal contact**.

### Claim 7

The **mosfet structure** of claim 6, wherein said **(ILD) gate oxide layer** is more than **(I)** eight times thicker than said **(SOX) substrate surface oxidation layer**.

### Claim 10

The **MOSFET structure** of claim 6, wherein said **(ML) material layer** is a metal contact layer providing external electrical contact with said at least one **(SR) source region**.

### Claim 11

The **MOSFET structure** of claim 10 wherein said **(ML) metal contact layer** extends over substantially the entire MOSFET structure except for at least one **(GC) gate contact access portion**,  
said **(ML) metal contact layer** being in electrical contact with said **at least one (SR) source region** but **electrically insulated from said at least two (GAT) polysilicon gates by** at least one of said **(ILD) gate oxide layer** and said substrate surface oxidation layer.

### Claim 12

The **MOSFET structure** of claim 10, wherein said **(ML) metal contact layer** extends over said **(GAT) gates and covers the space between them**,  
said **(ML) metal contact layer** being in electrical contact with said **at least one (SR) source region** but **electrically insulated from said (GAT) gates** by at least one of said **(ILD) gate oxide layer** and said substrate surface oxidation layer.

Claim 6

A **MOSFET structure**, comprising:

**SCTW90N65G2V**

Datasheet

Silicon carbide Power MOSFET 650 V, 119 A, 18 mΩ (typ.,  $T_J = 25^\circ\text{C}$ ) in an HiP247 package

**Features**

Order code	$V_{DS}$	$R_{DS(on)} \text{ max.}$	$I_D$
SCTW90N65G2V	650 V	24 mΩ	119 A

- Very high operating junction temperature capability ( $T_J = 200^\circ\text{C}$ )
- Very fast and robust intrinsic body diode
- Extremely low gate charge and input capacitances

**HIP247**

**Circuit Diagram**

**Applications**

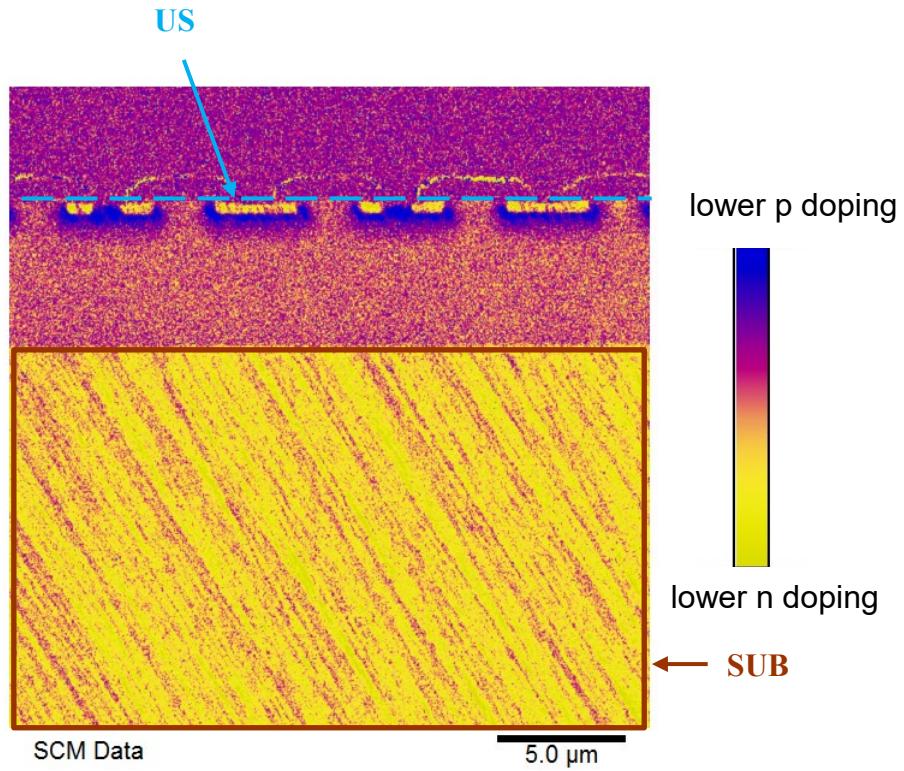
- Switching applications
- Power supply for renewable energy systems
- High frequency DC-DC converters

**Description**

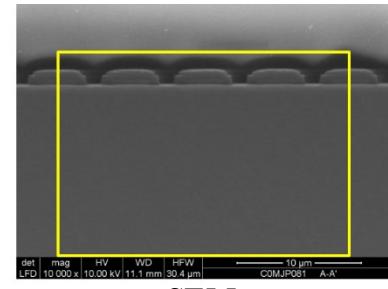
This silicon carbide Power MOSFET device has been developed using ST's advanced and innovative 2<sup>nd</sup> generation SiC MOSFET technology. The device features remarkably low on-resistance per unit area and very good switching performance. The variation of switching loss is almost independent of junction temperature.

Claim 6

a (SUB) silicon carbide wafer having a substrate body with an (US) upper surface,

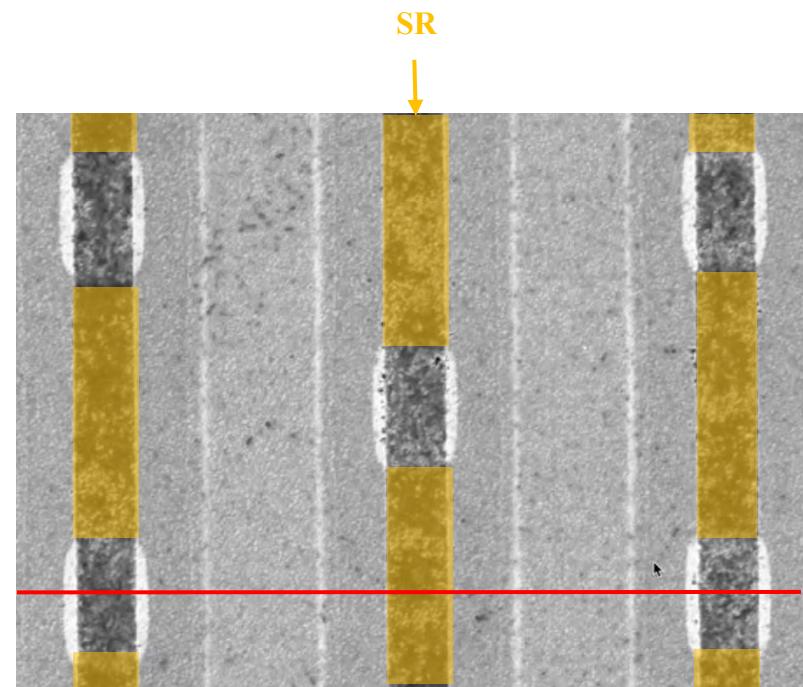


Note: Scanning Capacitance Microscopy (SCM) of the framed area in the Scanning Electron Microscopy (SEM) image.

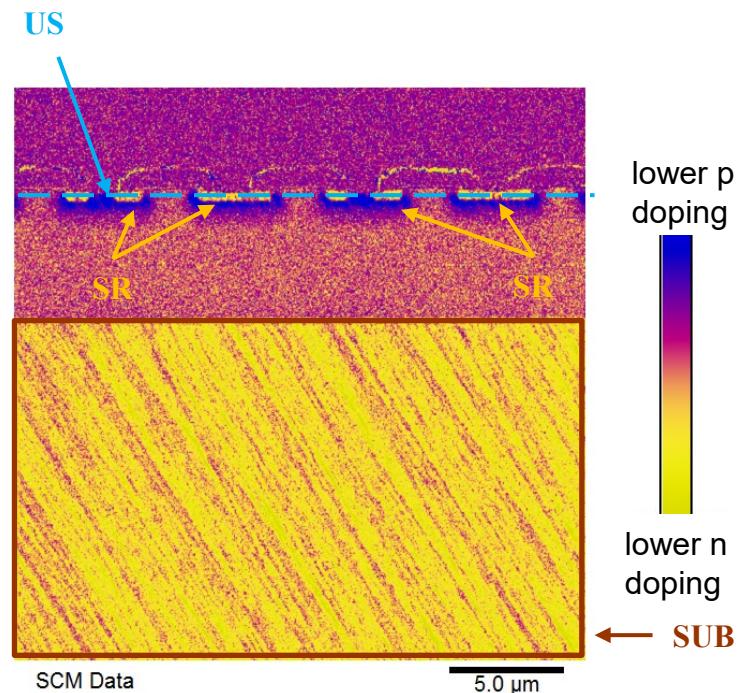


Claim 6

said **(SUB)** substrate body having **(SR)** at least one source region formed **(US)** adjacent said upper surface;



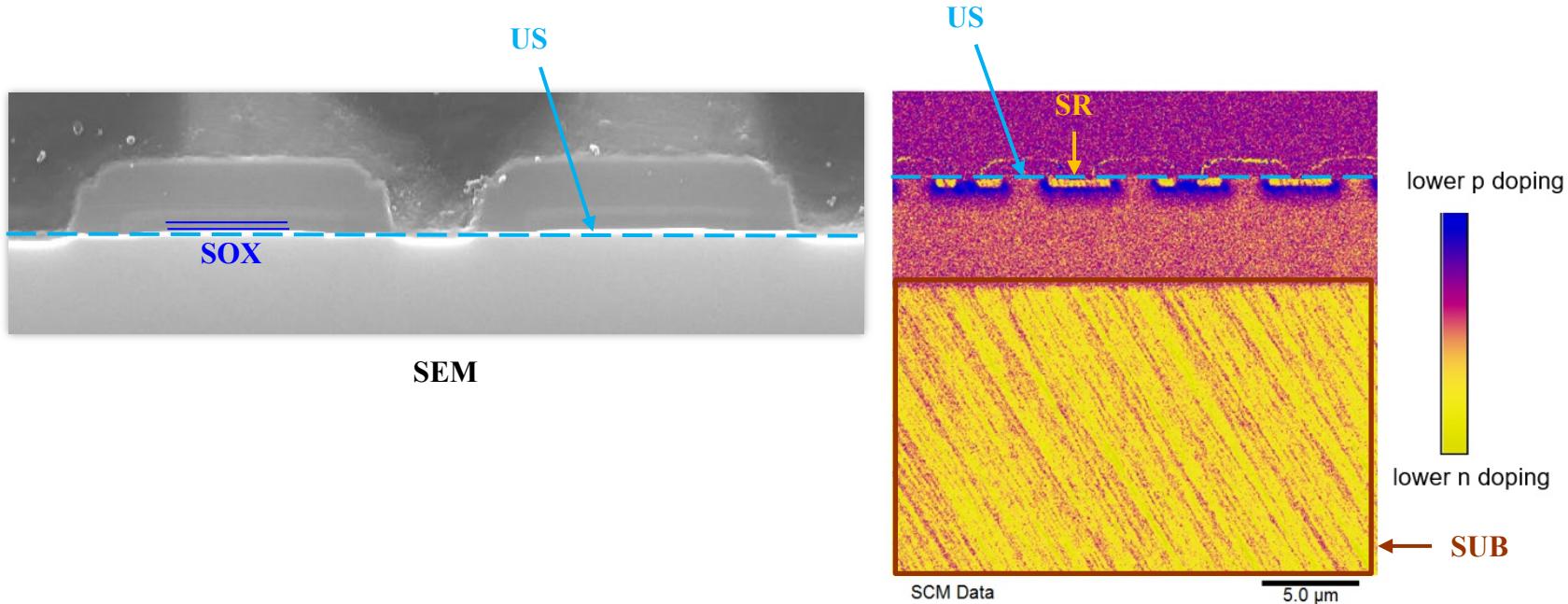
**Note:** Top-down view using Scanning Electron Microscopy Secondary Electron Potential Contrast (SEM SEPC), after polishing down to the silicon carbide.



**Note:** SCM view taken at A-A' cross section

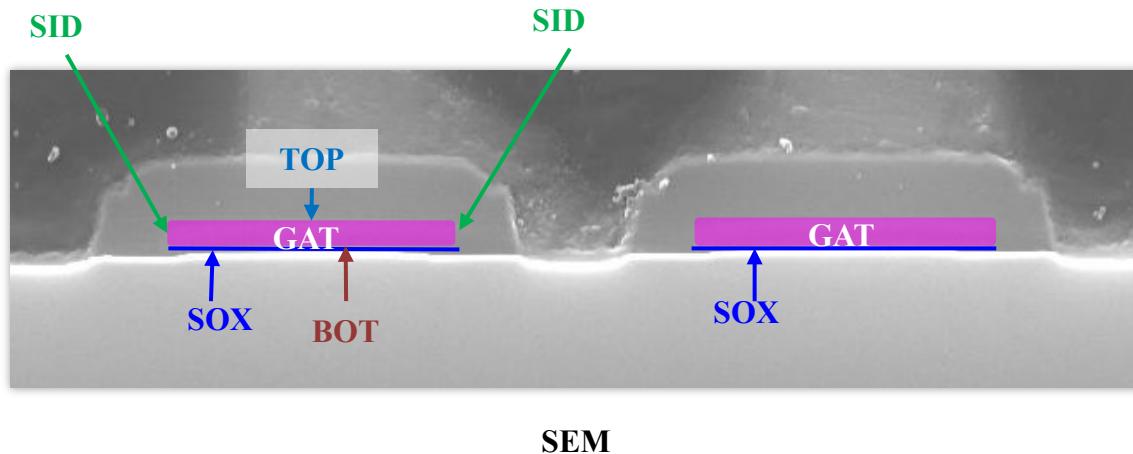
Claim 6

a (SOX) substrate surface oxidation layer on said (US) upper surface of said (SUB) substrate body and (SR) adjacent said source region;



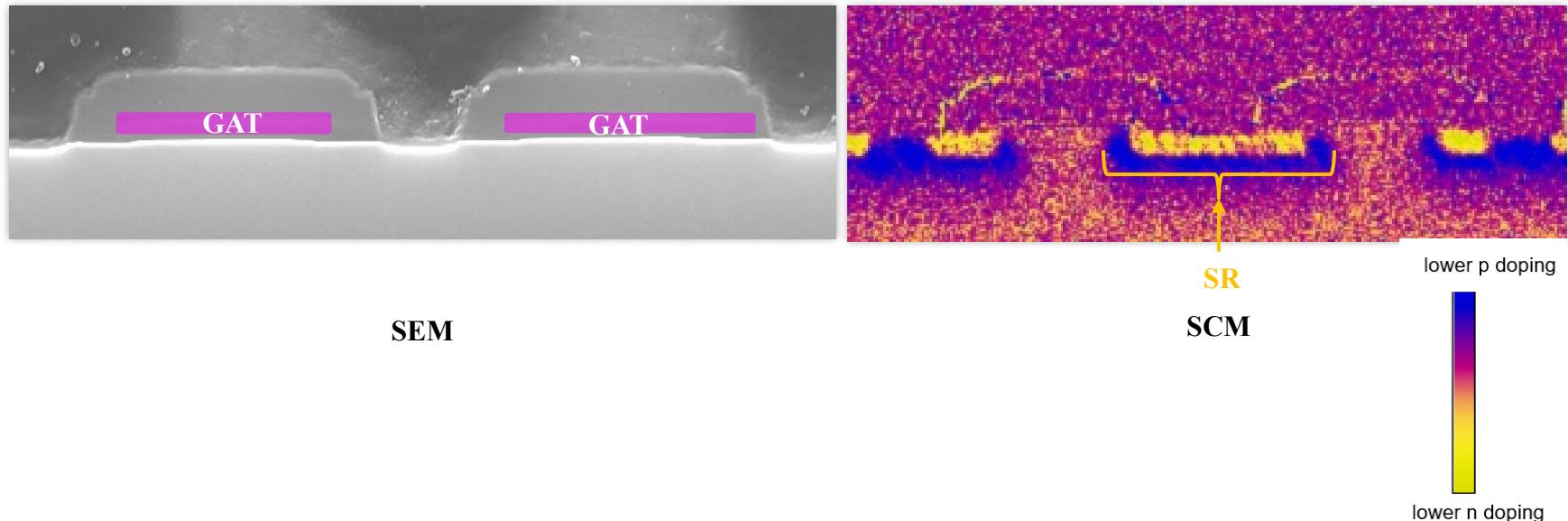
Claim 6

(GAT) at least two polysilicon gates above said (SOX) substrate surface oxidation layer, said (GAT) gates each having a (TOP) top, a (BOT) bottom and (SID) sides,



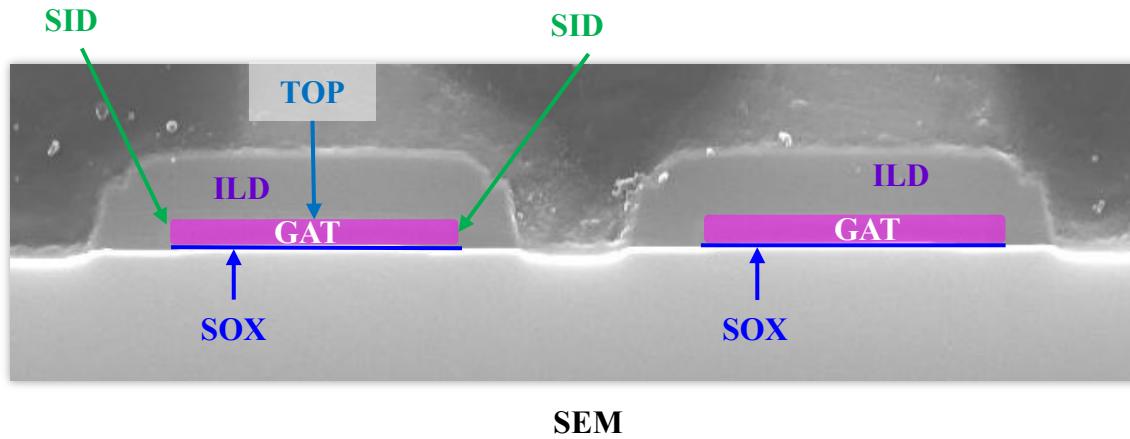
Claim 6

wherein a (SR) first source region of said at least one source region is juxtaposed between (GAT) first and second adjacent gates of said at least two polysilicon gates;



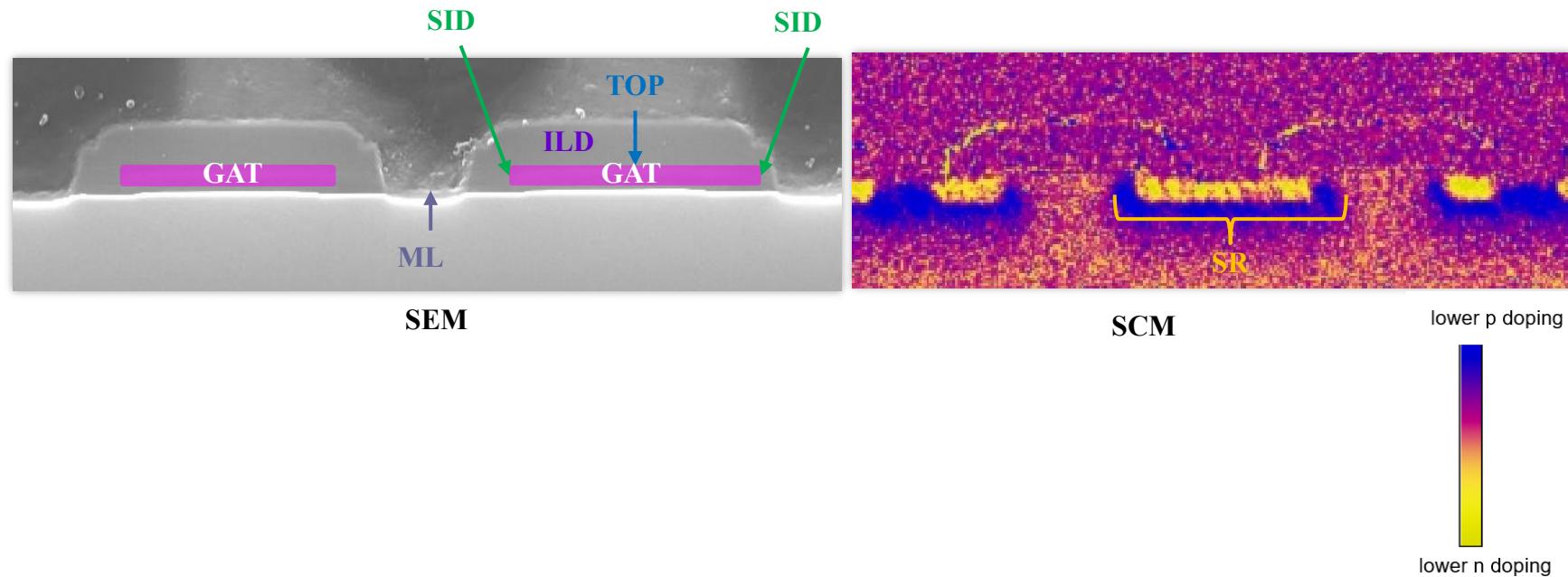
Claim 6

a (ILD) gate oxide layer, thicker than said (SOX) substrate surface oxidation layer, over said (TOP) tops and (SID) sides of (GAT) each of said gates; and



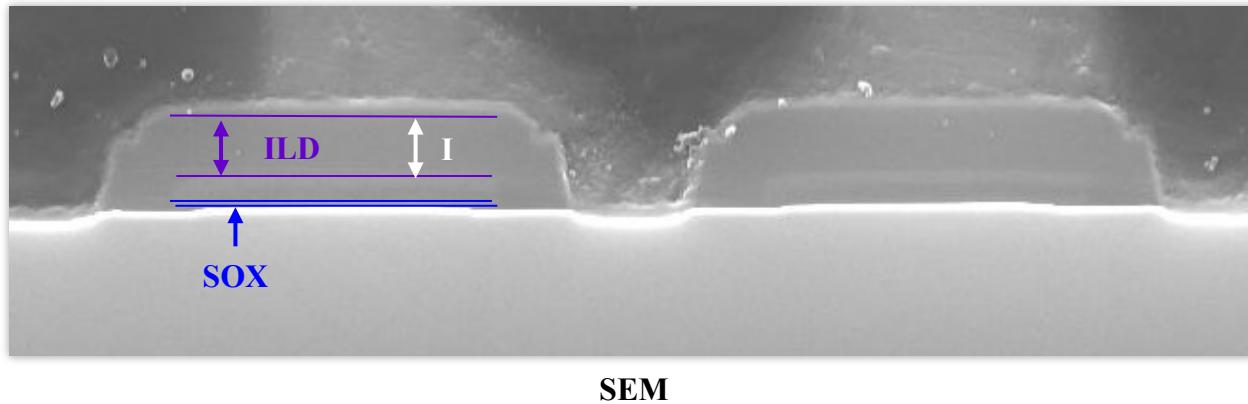
Claim 6

a (ML) material layer over said (SR) first source region and between said (ILD) gate oxide layers on said (SID) sides of said (GAT) gates, said (ML) material layer comprising one of an oxide and a (ML) metal contact.



Claim 7

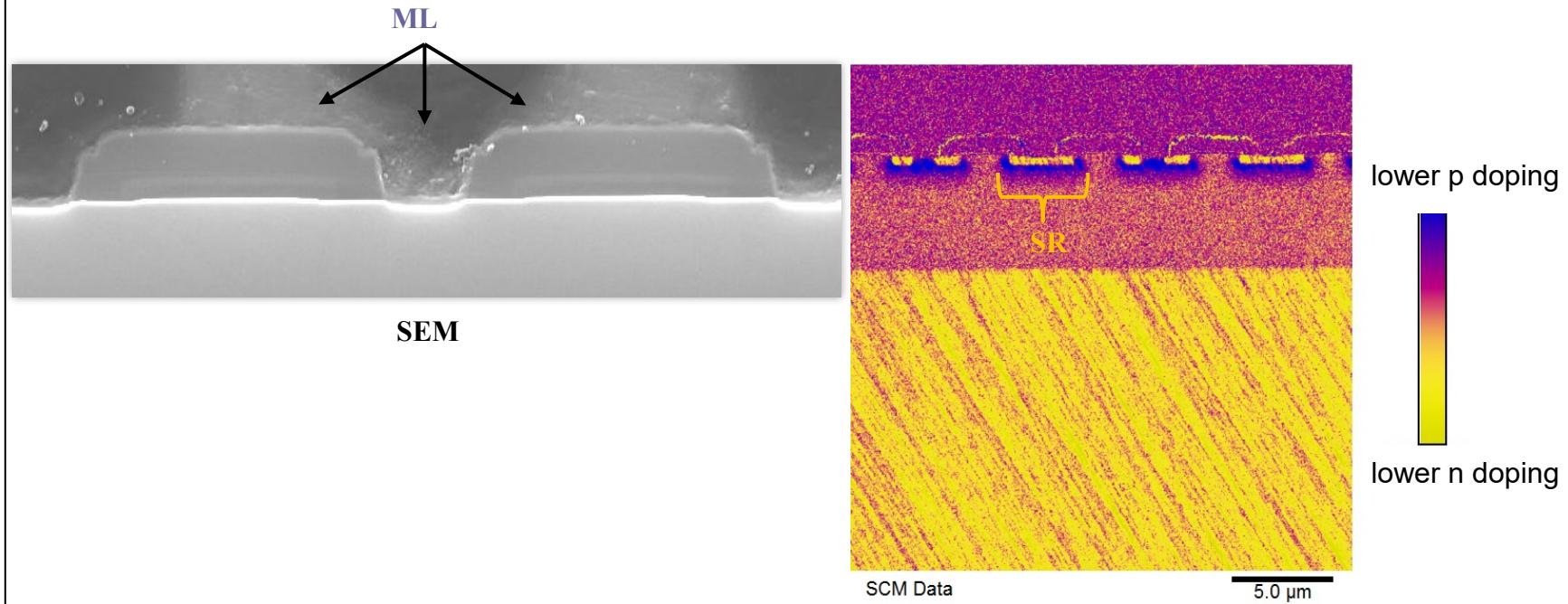
The mosfet structure of claim 6, wherein said **(ILD) gate oxide layer** is more than **(I)** eight times thicker than said **(SOX) substrate surface oxidation layer**.



SEM

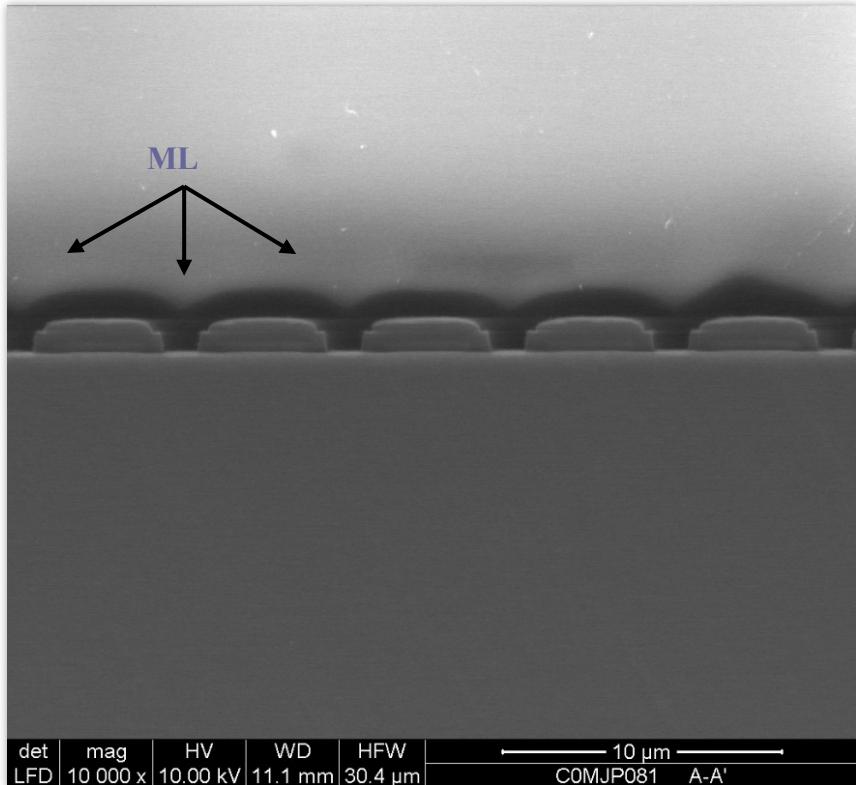
Claim 10

The **MOSFET structure** of claim 6, wherein said **(ML)** material layer is a metal contact layer providing external electrical contact with said at least one **(SR) source region**.



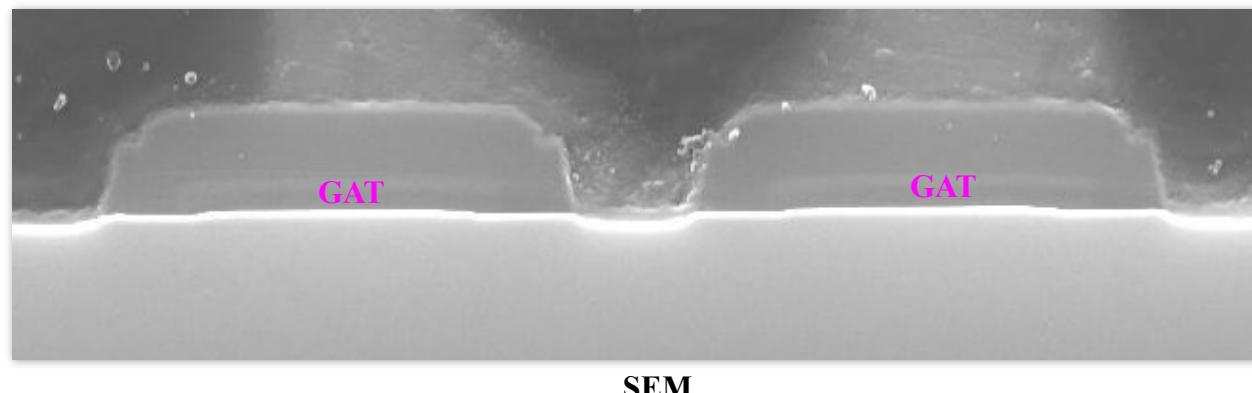
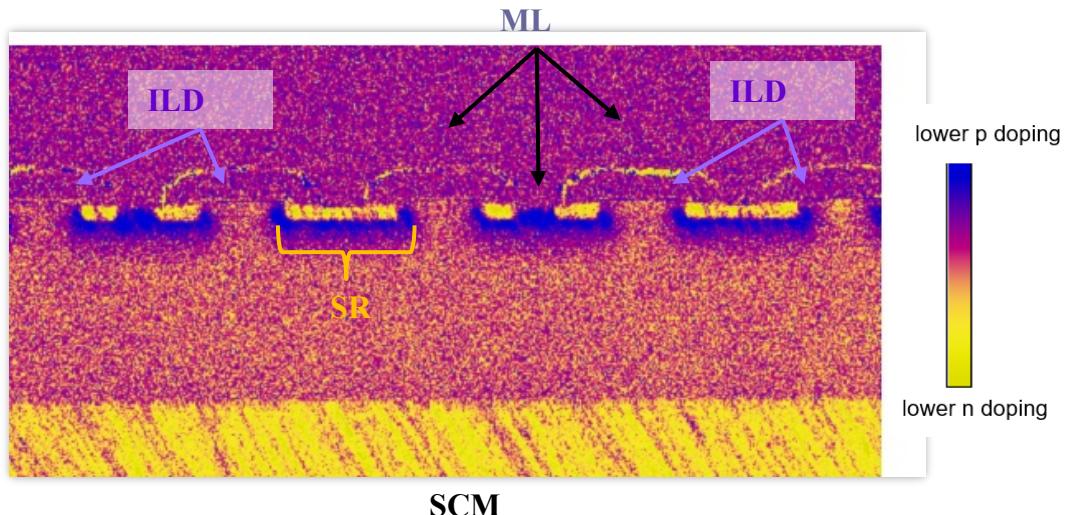
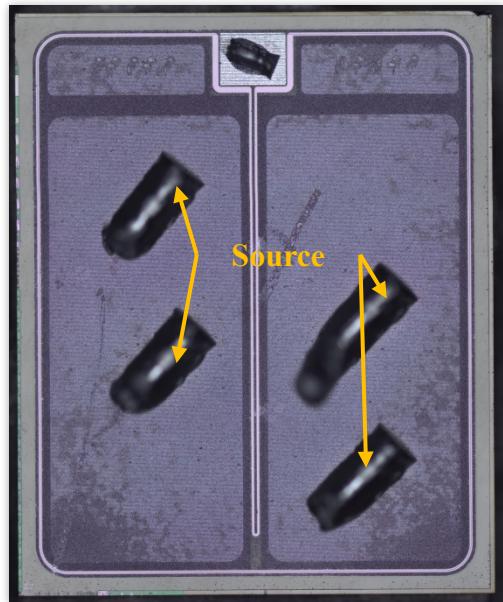
Claim 11

The **MOSFET structure** of claim 10 wherein said **(ML)** metal contact layer extends over substantially the entire **MOSFET structure** except for at least one **(GC)** gate contact access portion,



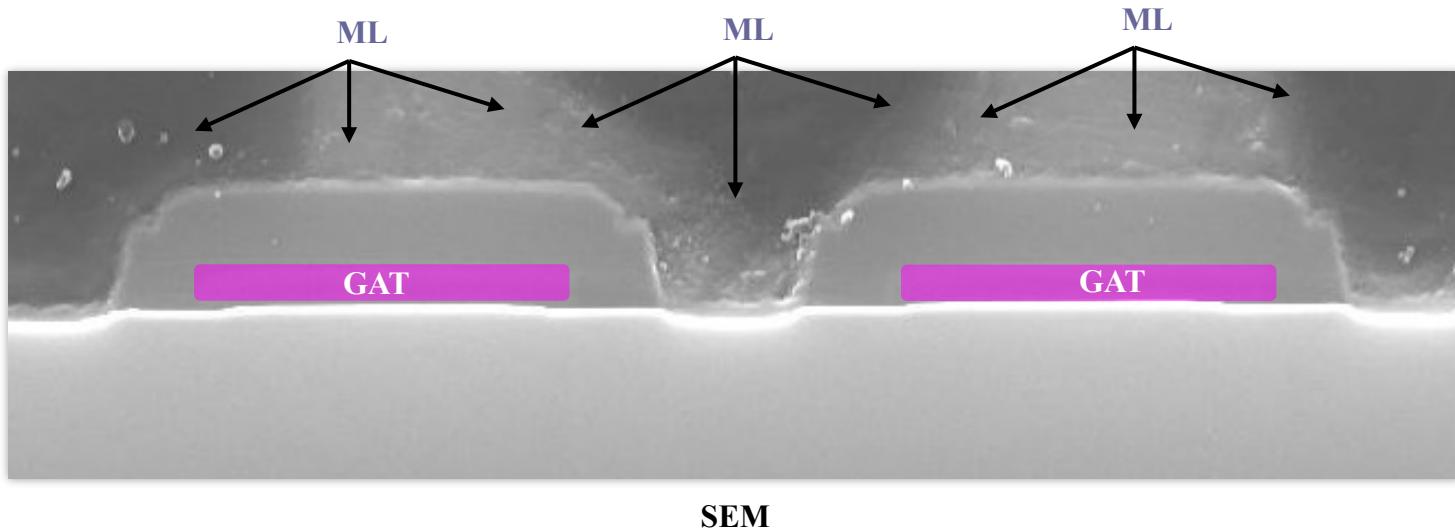
Claim 11

said (ML) metal contact layer being in electrical contact with said at least one (SR) source region but electrically insulated from said at least two (GAT) polysilicon gates by at least one of said (ILD) gate oxide layer and said substrate surface oxidation layer.



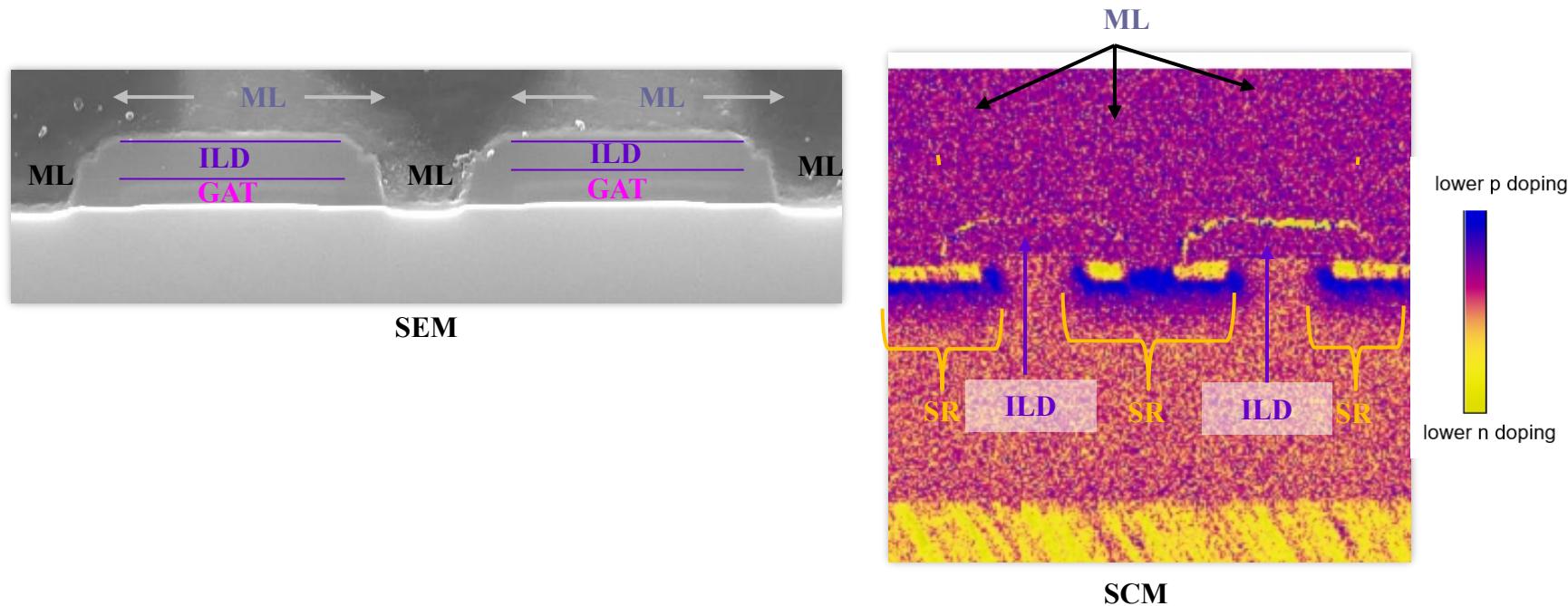
Claim 12

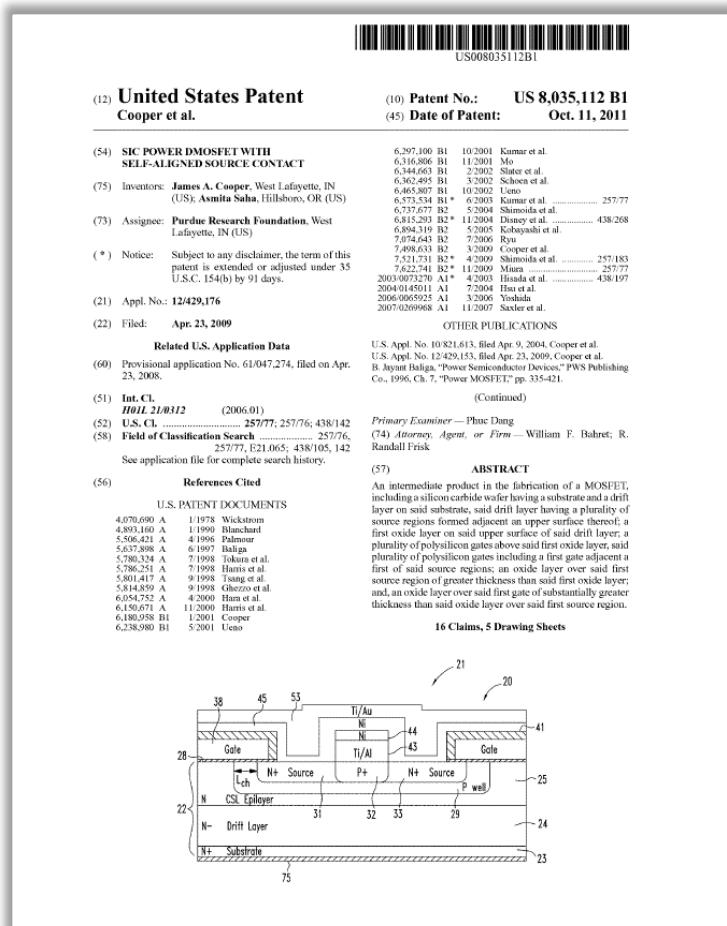
The **MOSFET structure** of claim 10, wherein said **(ML)** metal contact layer extends over said **(GAT)** gates and covers the space between them,



Claim 12

said (ML) metal contact layer being in electrical contact with said at least one (SR) source region but electrically insulated from said (GAT) gates by at least one of said (ILD) gate oxide layer and said substrate surface oxidation layer.





### Claim 6

A **mosfet structure**, comprising:

a **(SUB) silicon carbide wafer having a substrate body** with an **(US) upper surface**,  
said **(SUB) substrate body** having **(SR) at least one source region** formed **(US) adjacent said upper surface**;  
a **(SOX) substrate surface oxidation layer** on said **(US) upper surface** of said **(SUB) substrate body** and **(SR) adjacent said source region**;

**(GAT) at least two polysilicon gates** above said **(SOX) substrate surface oxidation layer**, said **(GAT) gates** each having a **(TOP) top**, a **(BOT) bottom** and **(SID) sides**, wherein a **(SR) first source region** of said **at least one source region** is juxtaposed between **(GAT) first and second adjacent gates** of said **at least two polysilicon gates**;

a **(ILD) gate oxide layer**, thicker than said **(SOX) substrate surface oxidation layer**, over said **(TOP) tops** and **(SID) sides** of **(GAT) each of said gates**; and

a **(ML) material layer** over said **(SR) first source region** and between said **(ILD) gate oxide layers** on said **(SID) sides** of said **(GAT) gates**,

said **(ML) material layer** comprising one of an oxide and a **(ML) metal contact**.

### Claim 7

The **mosfet structure** of claim 6, wherein said **(ILD) gate oxide layer** is more than **(I)** eight times thicker than said **(SOX) substrate surface oxidation layer**.

### Claim 10

The **MOSFET structure** of claim 6, wherein said **(ML) material layer** is a metal contact layer providing external electrical contact with said at least one **(SR) source region**.

### Claim 11

The **MOSFET structure** of claim 10 wherein said **(ML) metal contact layer** extends over substantially the entire MOSFET structure except for at least one **(GC) gate contact access portion**,  
said **(ML) metal contact layer** being in electrical contact with said **at least one (SR) source region** but **electrically insulated from said at least two (GAT) polysilicon gates by** at least one of said **(ILD) gate oxide layer** and said substrate surface oxidation layer.

### Claim 12

The **MOSFET structure** of claim 10, wherein said **(ML) metal contact layer** extends over said **(GAT) gates and covers the space between them**,  
said **(ML) metal contact layer** being in electrical contact with said **at least one (SR) source region** but **electrically insulated from said (GAT) gates** by at least one of said **(ILD) gate oxide layer** and said substrate surface oxidation layer.

Claim 6

A MOSFET structure, comprising:

**SCTW70N120G2V**  
Datasheet

Silicon carbide Power MOSFET 1200 V, 91 A, 21 mΩ (typ.,  $T_J = 25^\circ\text{C}$ )  
in an HiP247 package

**Features**

Order code	$V_{DS}$	$R_{DS(on)} \text{ typ.}$	$I_D$
SCTW70N120G2V	1200 V	21 mΩ	91 A

- Very high operating junction temperature capability ( $T_J = 200^\circ\text{C}$ )
- Very fast and robust intrinsic body diode
- Extremely low gate charge and input capacitances

**Applications**

- Charger
- Power supply for renewable energy systems
- High frequency DC-DC converters

**Description**

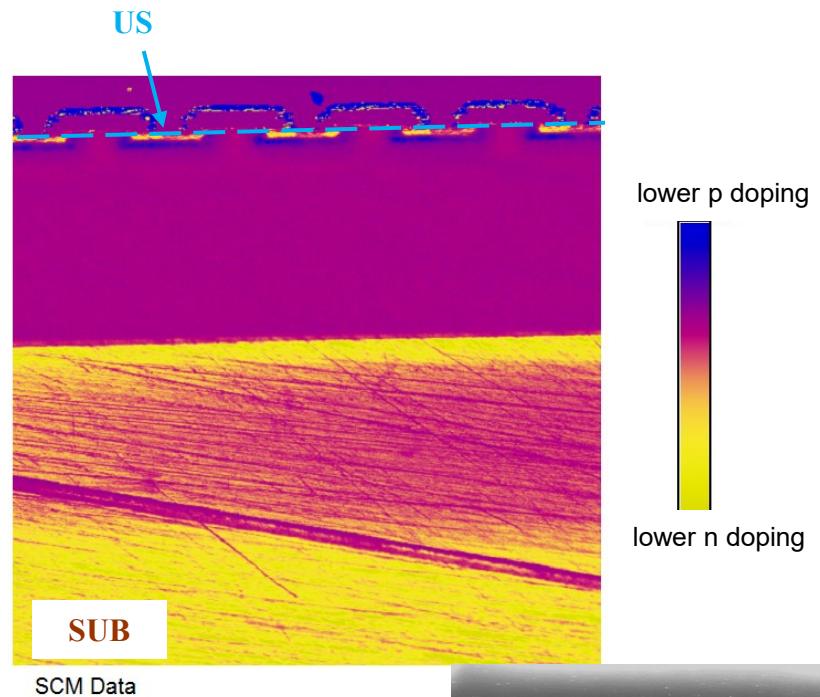
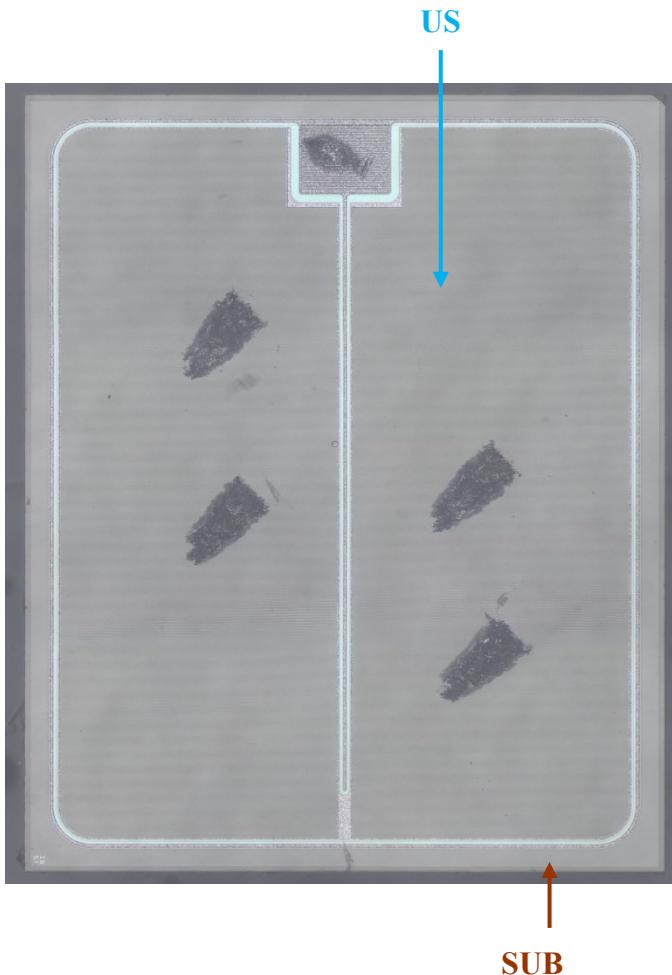
This silicon carbide Power MOSFET is produced exploiting the advanced, innovative properties of wide bandgap materials. This results in unsurpassed on-resistance per unit area and very good switching performance almost independent of temperature. The outstanding thermal properties of the SiC material allow designers to use an industry-standard outline with significantly improved thermal capability. These features render the device perfectly suitable for high-efficiency and high power density applications.

HiP247

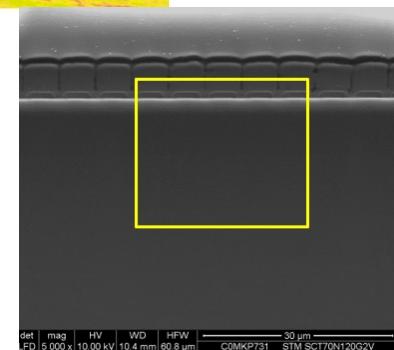
AM0147sv1\_noZen

Claim 6

a (SUB) silicon carbide wafer having a substrate body with an (US) upper surface,



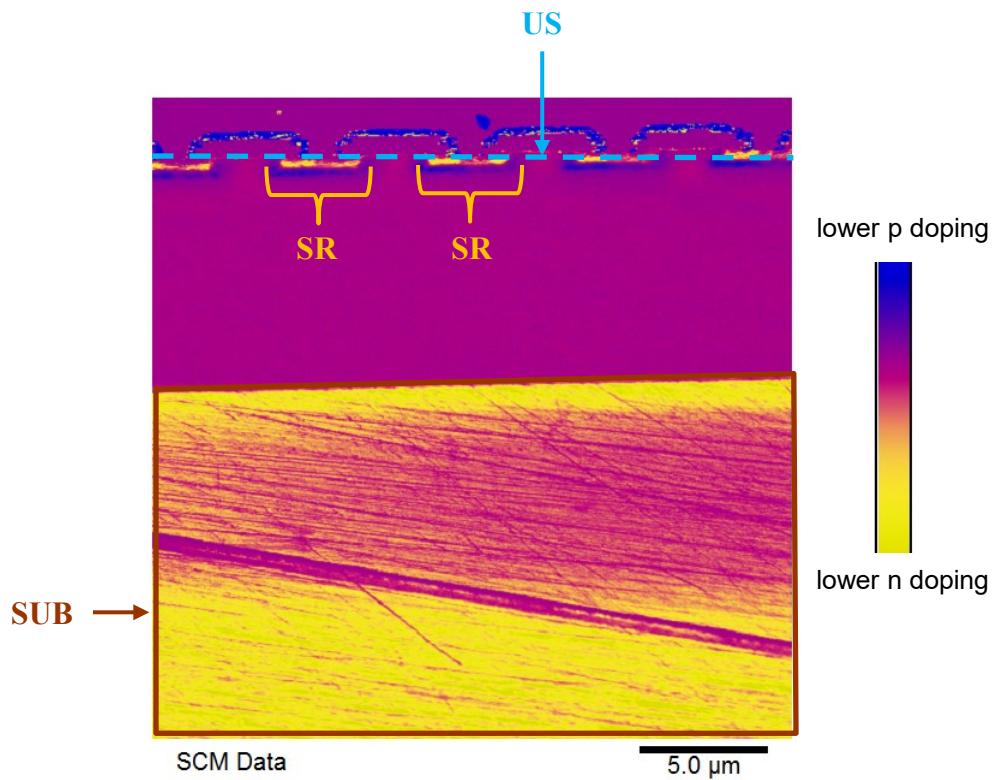
**Note:** Scanning Capacitance Microscopy (SCM) of the framed area in the Scanning Electron Microscopy (SEM) image.



SEM

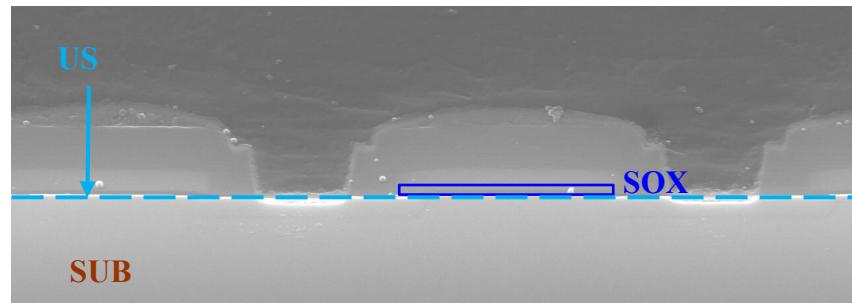
Claim 6

said **(SUB)** substrate body having **(SR)** at least one source region formed **(US)** adjacent said upper surface;

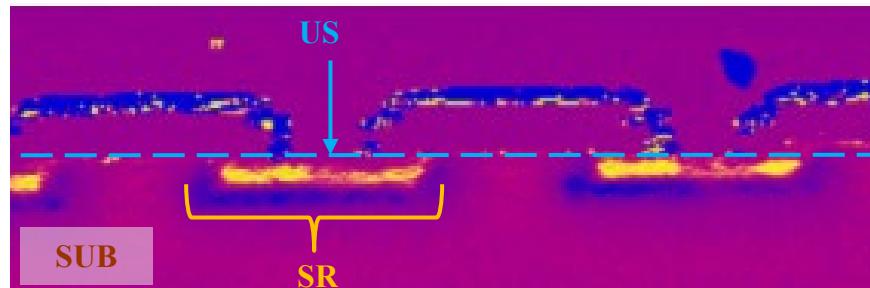


Claim 6

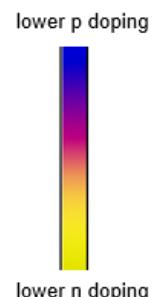
a (SOX) substrate surface oxidation layer on said (US) upper surface of said (SUB) substrate body and (SR) adjacent said source region;



SEM

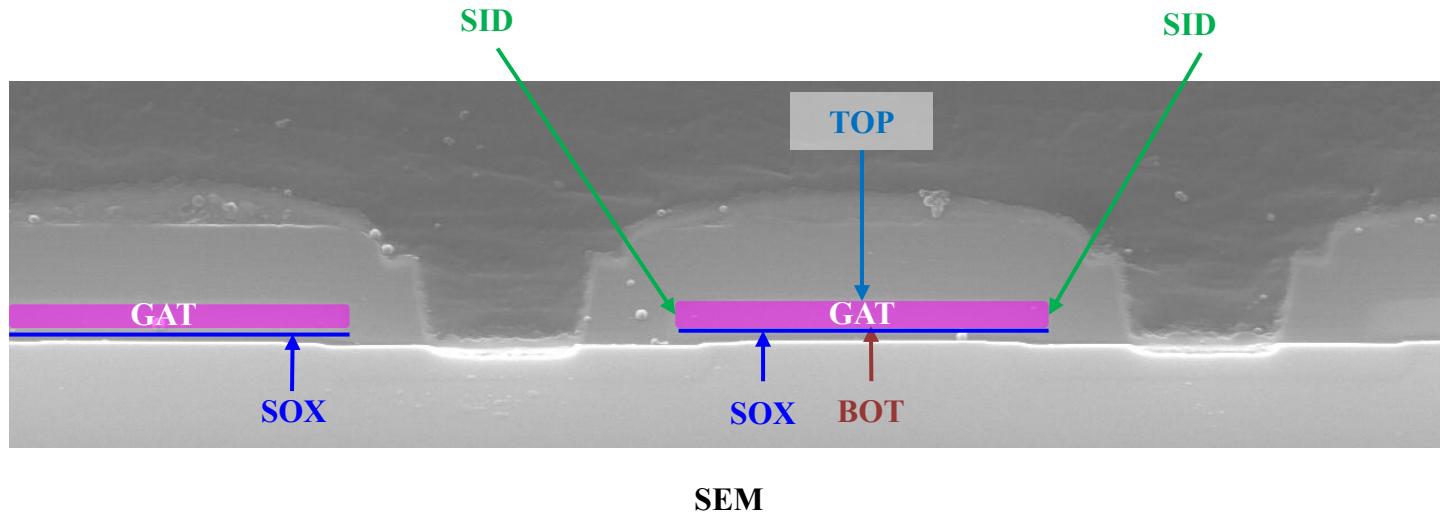


SCM



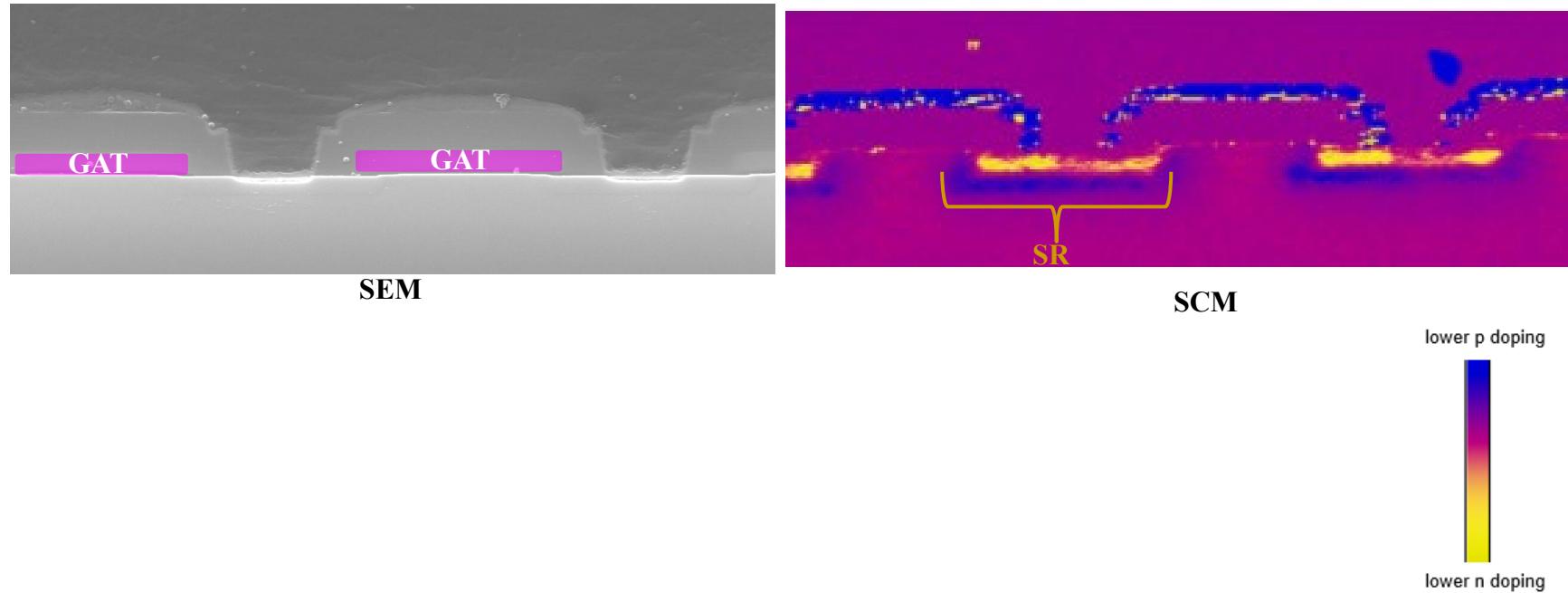
Claim 6

(GAT) at least two polysilicon gates above said (SOX) substrate surface oxidation layer, said (GAT) gates each having a (TOP) top, a (BOT) bottom and (SID) sides,



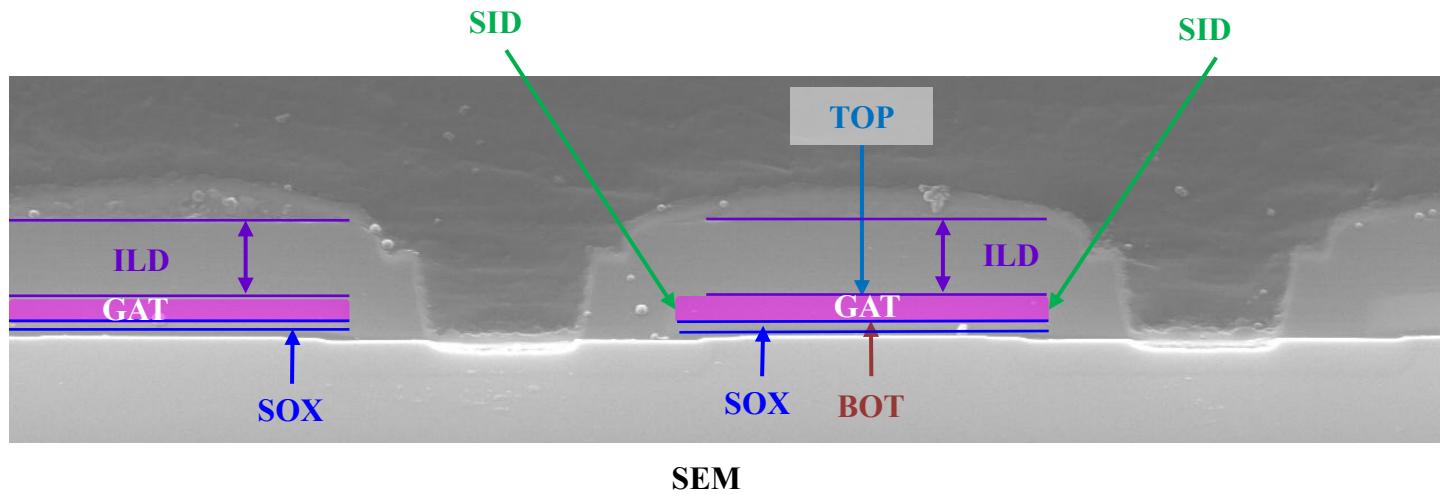
Claim 6

wherein a (SR) first source region of said at least one source region is juxtaposed between (GAT) first and second adjacent gates of said at least two polysilicon gates;



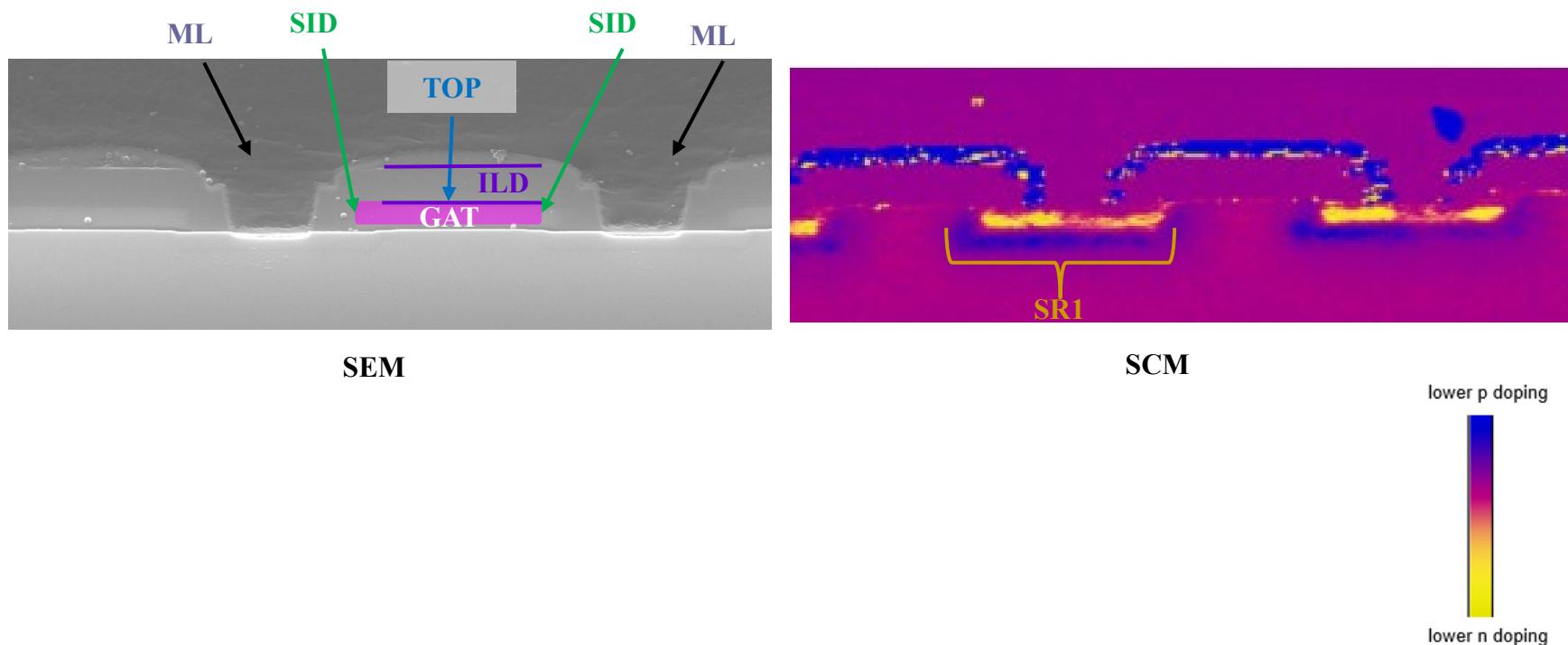
Claim 6

a (ILD) gate oxide layer, thicker than said (SOX) substrate surface oxidation layer, over said (TOP) tops and (SID) sides of (GAT) each of said gates; and



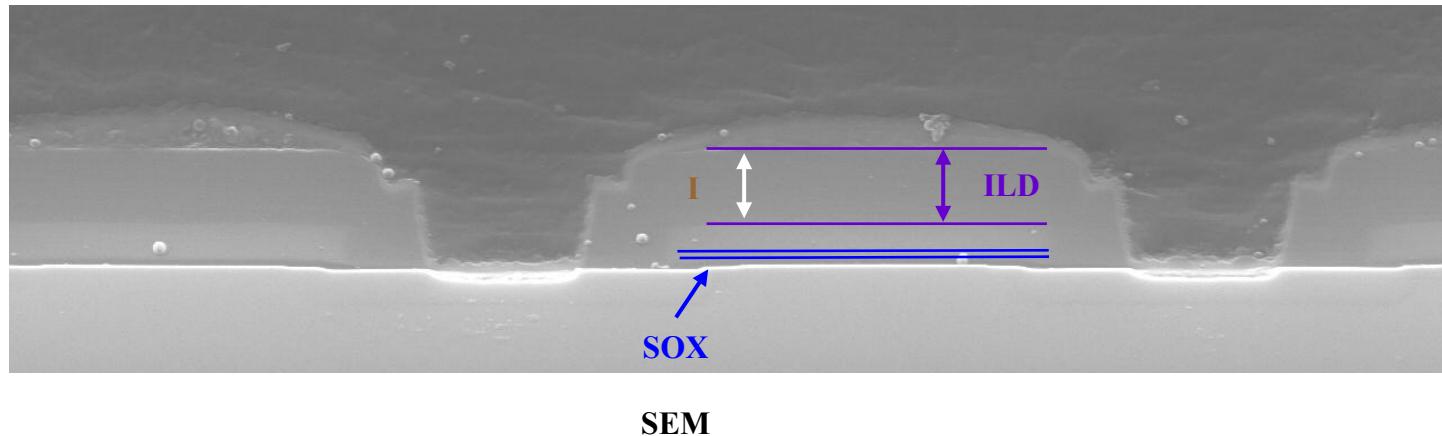
Claim 6

a (ML) material layer over said (SR1) first source region and between said (ILD) gate oxide layers on said (SID) sides of said (GAT) gates, said (ML) material layer comprising one of an oxide and a (ML) metal contact.



Claim 7

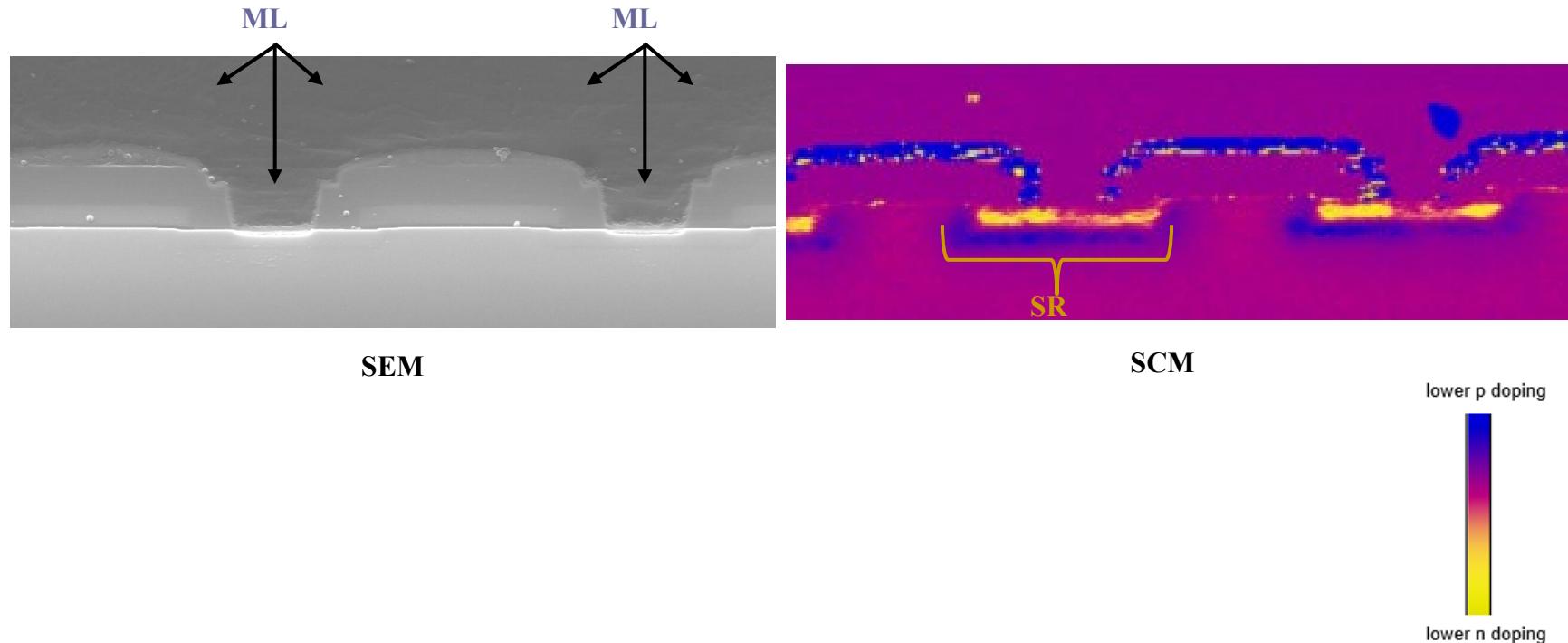
The mosfet structure of claim 6, wherein said **(ILD) gate oxide layer** is more than **(I)** eight times thicker than said **(SOX) substrate surface oxidation layer**.



SEM

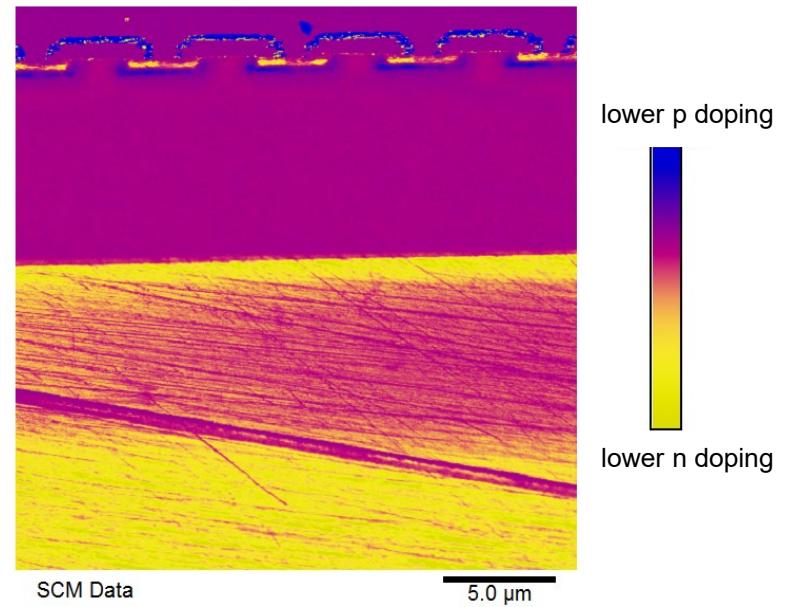
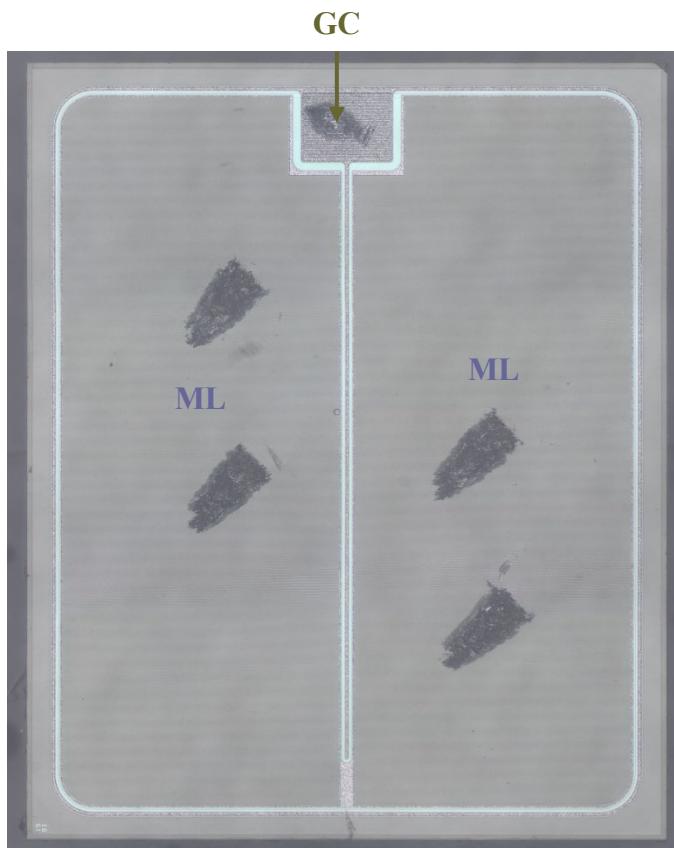
Claim 10

The **MOSFET structure** of claim 6, wherein said **(ML)** material layer is a metal contact layer providing external electrical contact with said at least one **(SR) source region**.



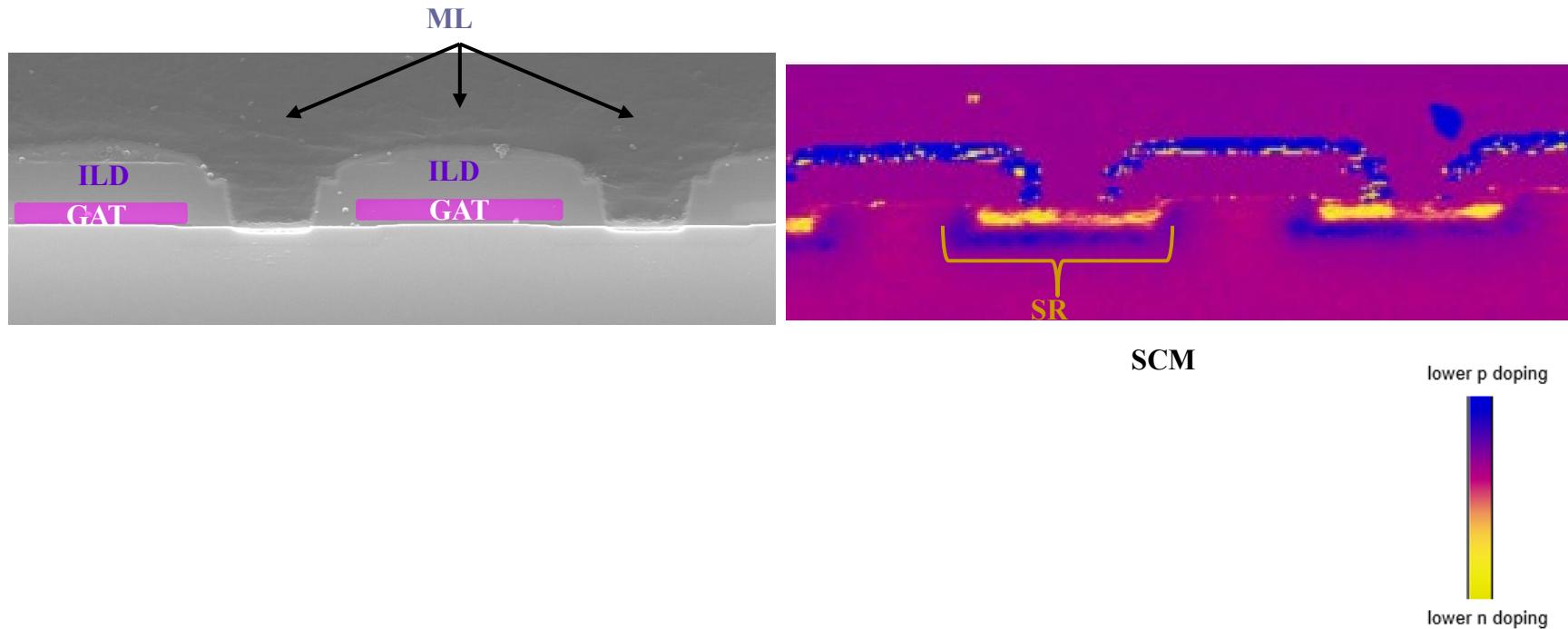
Claim 11

The **MOSFET structure** of claim 10 wherein said **(ML)** metal contact layer extends over substantially the entire **MOSFET structure** except for at least one **(GC)** gate contact access portion,



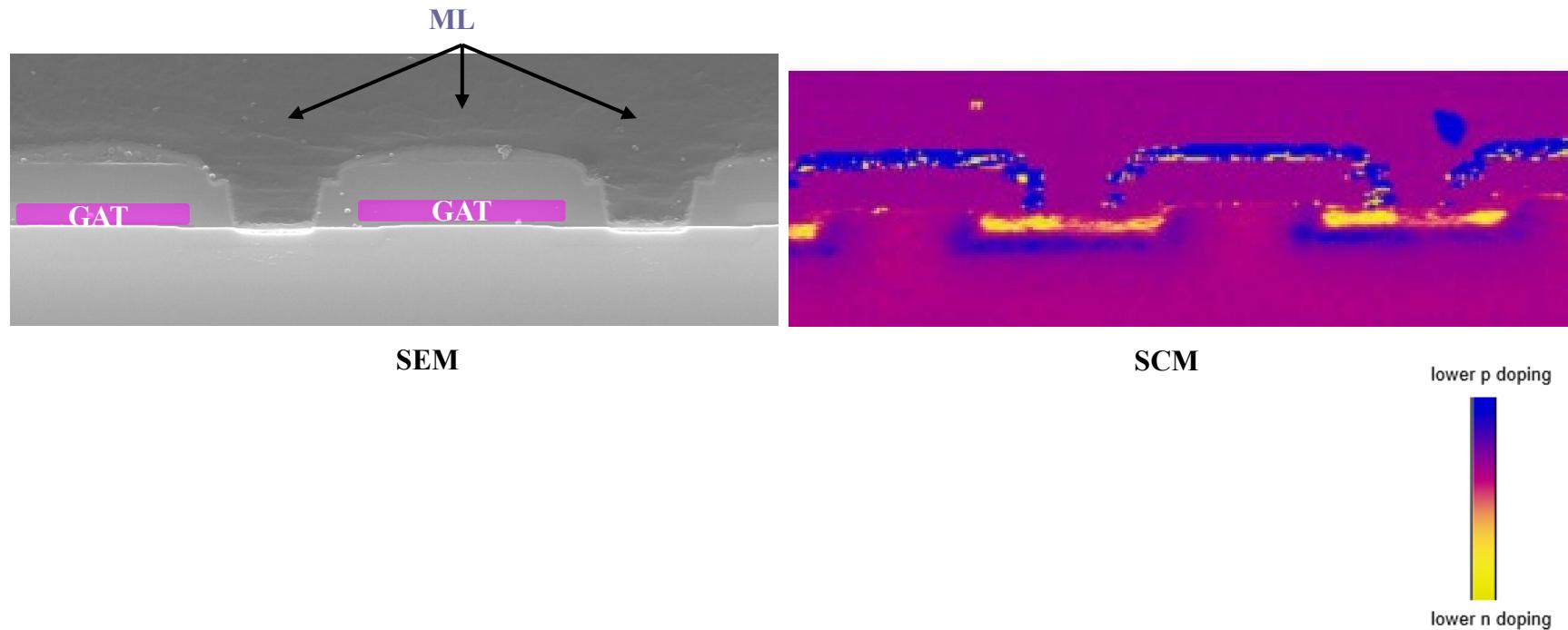
Claim 11

said (ML) metal contact layer being in electrical contact with said at least one (SR) source region but electrically insulated from said at least two (GAT) polysilicon gates by at least one of said (ILD) gate oxide layer and said substrate surface oxidation layer.



Claim 12

The **MOSFET structure** of claim 10, wherein said **(ML)** metal contact layer extends over said **(GAT)** gates and covers the space between them,



Claim 12

said (ML) metal contact layer being in electrical contact with said at least one (SR) source region but electrically insulated from said (GAT) gates by at least one of said (ILD) gate oxide layer and said substrate surface oxidation layer.

